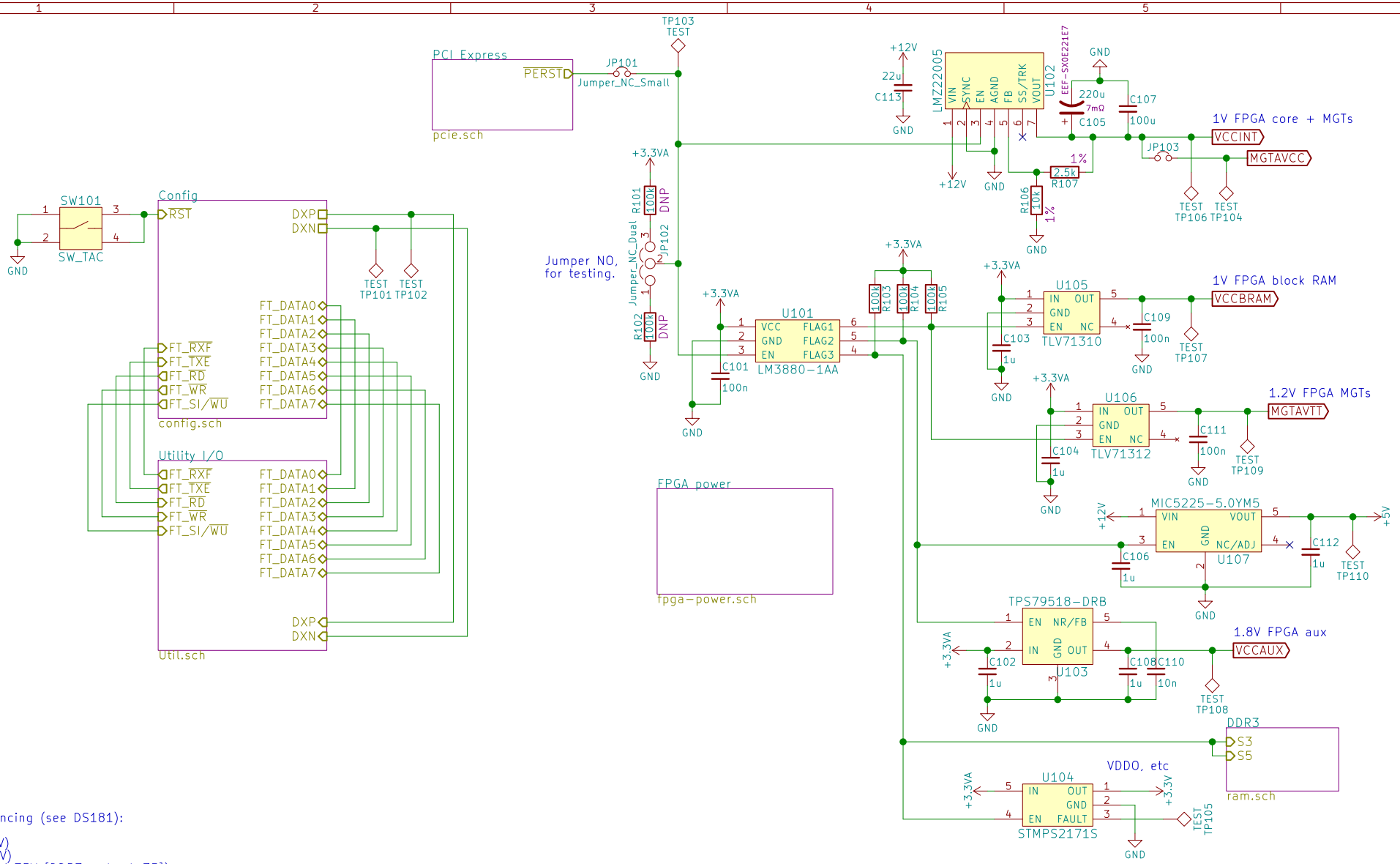


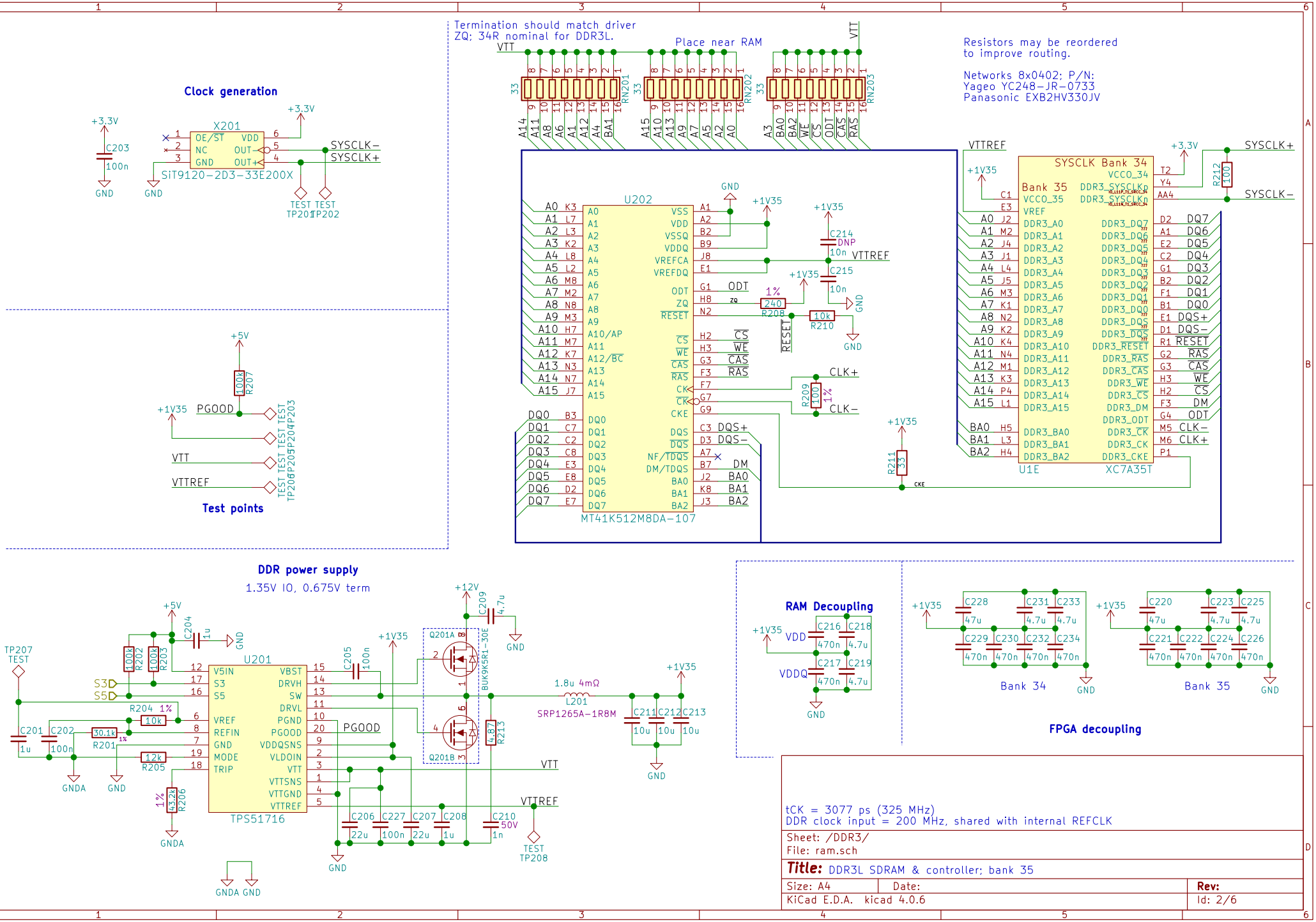
Power sequencing (see DS181):
VCCINT (1V)
VCCBRAM (1V)
VCCAUX (1.8V)
VCCO (3.3V, 1.35V [DDR3 @ bank 35])

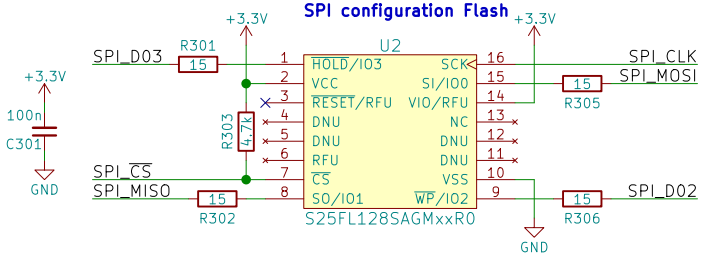
VCCINT + MGTAVCC (1V)
MGTAVTT (1.2V)

4.7u and smaller decoupling caps:
place within 2" of FPGA; closer better.
Minimize inductance, see
Xilinx UG483 chapter 2

Unless otherwise noted, ceramic
(X5R, X7R) capacitors acceptable.

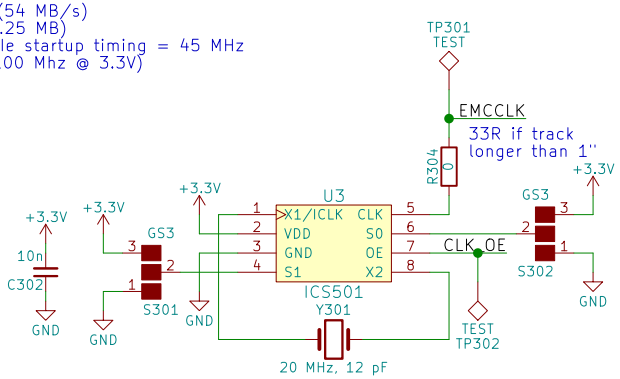
Sheet: /		
File: pcie-memorydumper.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.6		Id: 1/6


Clock generation
X201
SiT9120-2D3-33E200X
SYSCLK-
SYSCLK+
Test points
Termination should match driver
ZQ; 34R nominal for DDR3L.
Place near RAM
Resistors may be reordered
to improve routing.
Networks 8x0402; P/N:
Yageo YC248-JR-0733
Panasonic EXB2HV330JV
U202
MT41K512M8DA-107
U1E
XC7A35T
SYSCLK Bank 34
Bank 35
DDR power supply
1.35V IO, 0.675V term
U201
TPS51716
L201
SRP1265A-1R8M
RAM Decoupling
FPGA decoupling
Bank 34
Bank 35
tCK = 3077 ps (325 MHz)
DDR clock input = 200 MHz, shared with internal REFCLK
Sheet: /DDR3/
File: ram.sch
Title: DDR3L SDRAM & controller; bank 35
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 4.0.6
Id: 2/6

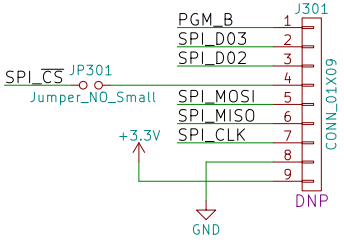


See AN201383 for routing guidelines.
Length match clock/data.

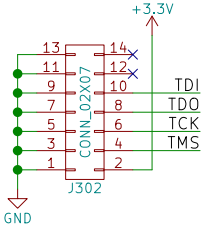
SPI flash up to 108 MHz (54 MB/s)
FPGA bitstream ~18 Mb (2.25 MB)
Minimum frequency for PCIe startup timing = 45 MHz
(S1, S0) = ... (F_max = 100 Mhz @ 3.3V)
(0, 0) => 80 MHz
(0, 1) => 100 MHz
(Z, 1) => 62.5 MHz
(1, Z) => 60 MHz



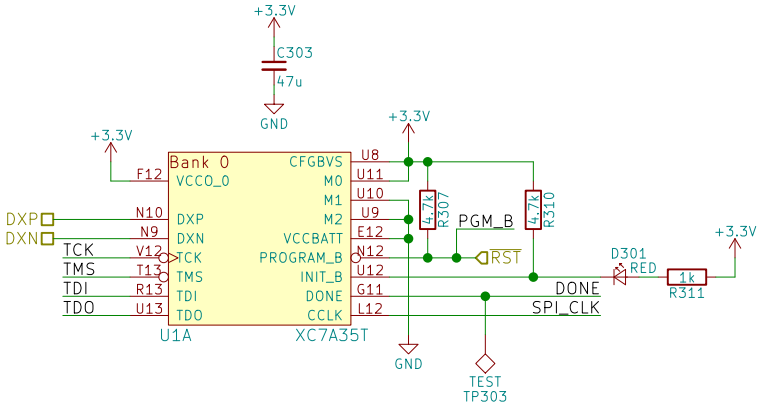
EMCCLK source



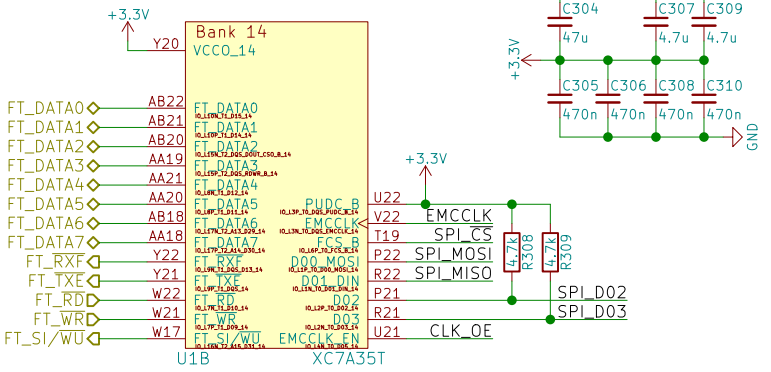
SPI flash programming interface



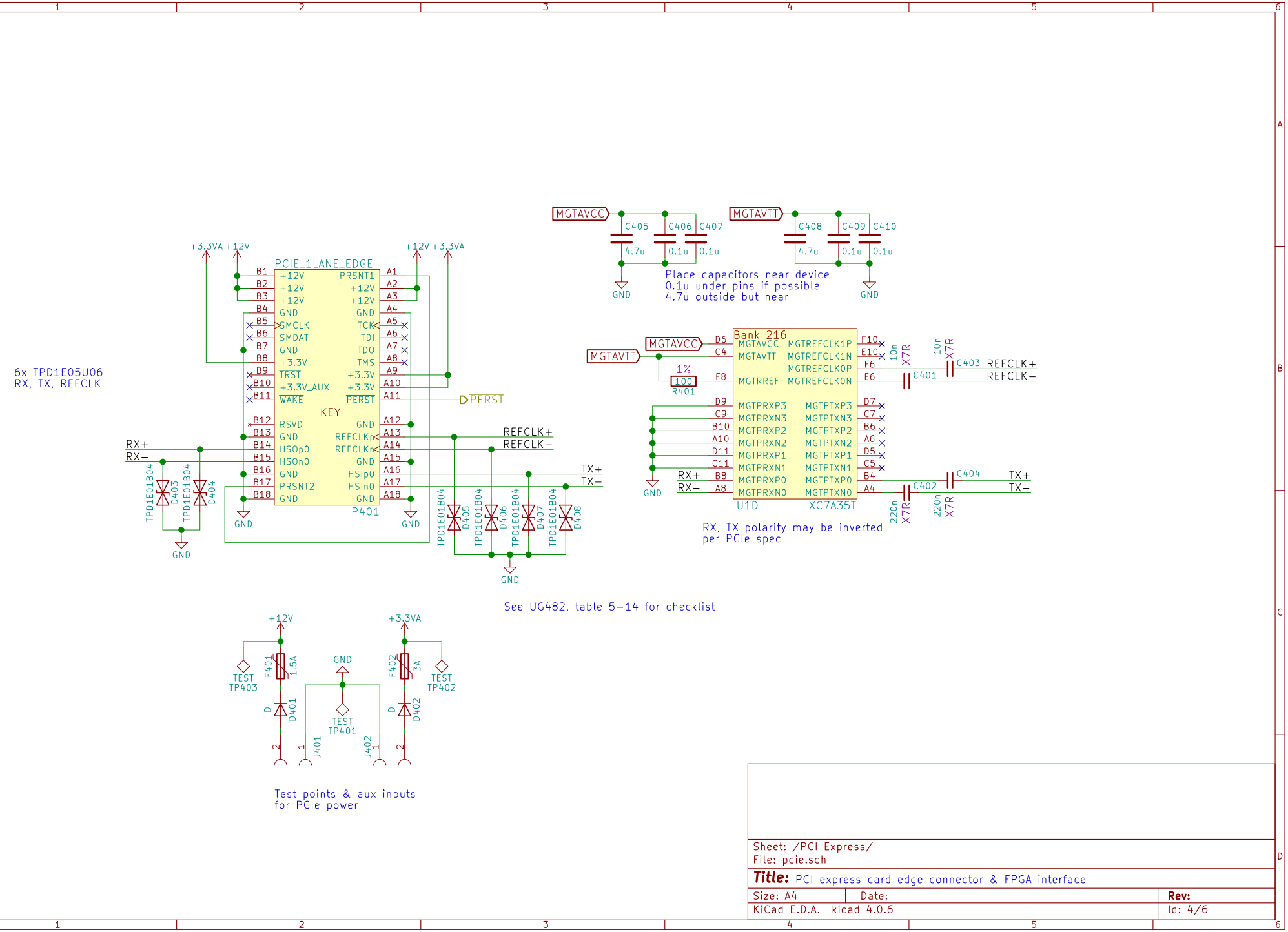
Xilinx Platform Cable connector
Molex 87831-1420
FCI 98414-G06-14

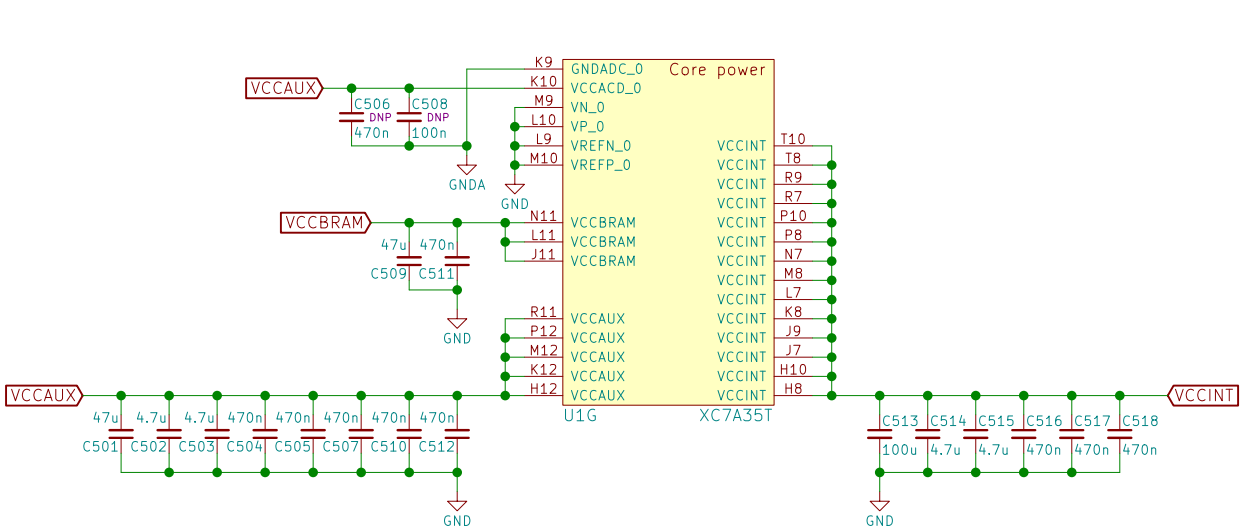


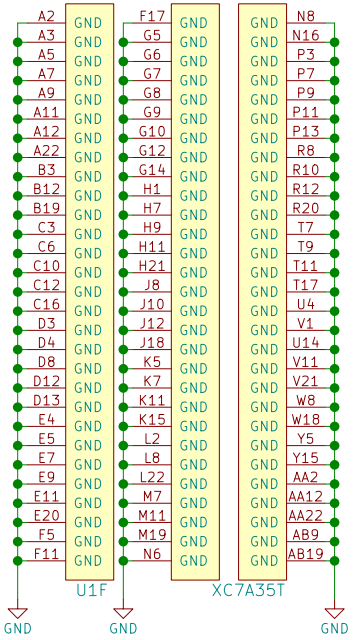
FPGA configuration interface



Sheet: /Config/		
File: config.sch		
Title: FPGA configuration interface & JTAG		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.6		Id: 3/6


6x TPD1E05U06
RX, TX, REFCLK
PCIE_1LANE_EDGE
+3.3VA +12V
+12V +3.3VA
B1 +12V
B2 +12V
B3 +12V
B4 GND
B5 SMCLK
B6 SMDAT
B7 GND
B8 +3.3V
B9 TRST
B10 +3.3V_AUX
B11 WAKE
KEY
B12 RSVD
B13 GND
B14 HSOp0
B15 HSOn0
B16 GND
B17 PRSNT2
B18 GND
A1 PRSNT1
A2 +12V
A3 +12V
A4 GND
A5 TCK
A6 TDI
A7 TDO
A8 TMS
A9 +3.3V
A10 +3.3V
A11 PERST
A12 GND
A13 REFCLKp
A14 REFCLKn
A15 GND
A16 HSIp0
A17 HSIn0
A18 GND
P401
PERST
REFCLK+
REFCLK−
TX+
TX−
RX+
RX−
TPD1E01B04
D403
D404
D405
D406
D407
D408
GND
MGTAVCC
MGTAVTT
C405 4.7u
C406 0.1u
C407 0.1u
C408 4.7u
C409 0.1u
C410 0.1u
Place capacitors near device
0.1u under pins if possible
4.7u outside but near
Bank 216
D6 MGTAVCC
C4 MGTAVTT
MGTRREF
1%
100
R401
MGTREFCLK1P
MGTREFCLK1N
MGTREFCLK0P
MGTREFCLK0N
D9 MGTPRXP3
C9 MGTPRXN3
B10 MGTPRXP2
A10 MGTPRXN2
D11 MGTPRXP1
C11 MGTPRXN1
B8 MGTPRXP0
A8 MGTPRXN0
MGTPTXP3 D7
MGTPTXN3 C7
MGTPTXP2 B6
MGTPTXN2 A6
MGTPTXP1 D5
MGTPTXN1 C5
MGTPTXP0 B4
MGTPTXN0 A4
F10
E10
F6
E6
10n X7R
C403
C401
C404
C402
220n X7R
U1D XC7A35T
RX, TX polarity may be inverted
per PCIe spec
See UG482, table 5−14 for checklist
+12V
+3.3VA
TEST TP403
TEST TP402
TEST TP401
F401 1.5A
F402 3A
D401
D402
J401
J402
Test points & aux inputs
for PCIe power
Sheet: /PCI Express/
File: pcie.sch
Title: PCI express card edge connector & FPGA interface
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 4.0.6
Id: 4/6





THE SHEET OF POWER

Sheet: /FPGA power/
File: fpga-power.sch

Title:

Size: A4	Date:	**Rev:**
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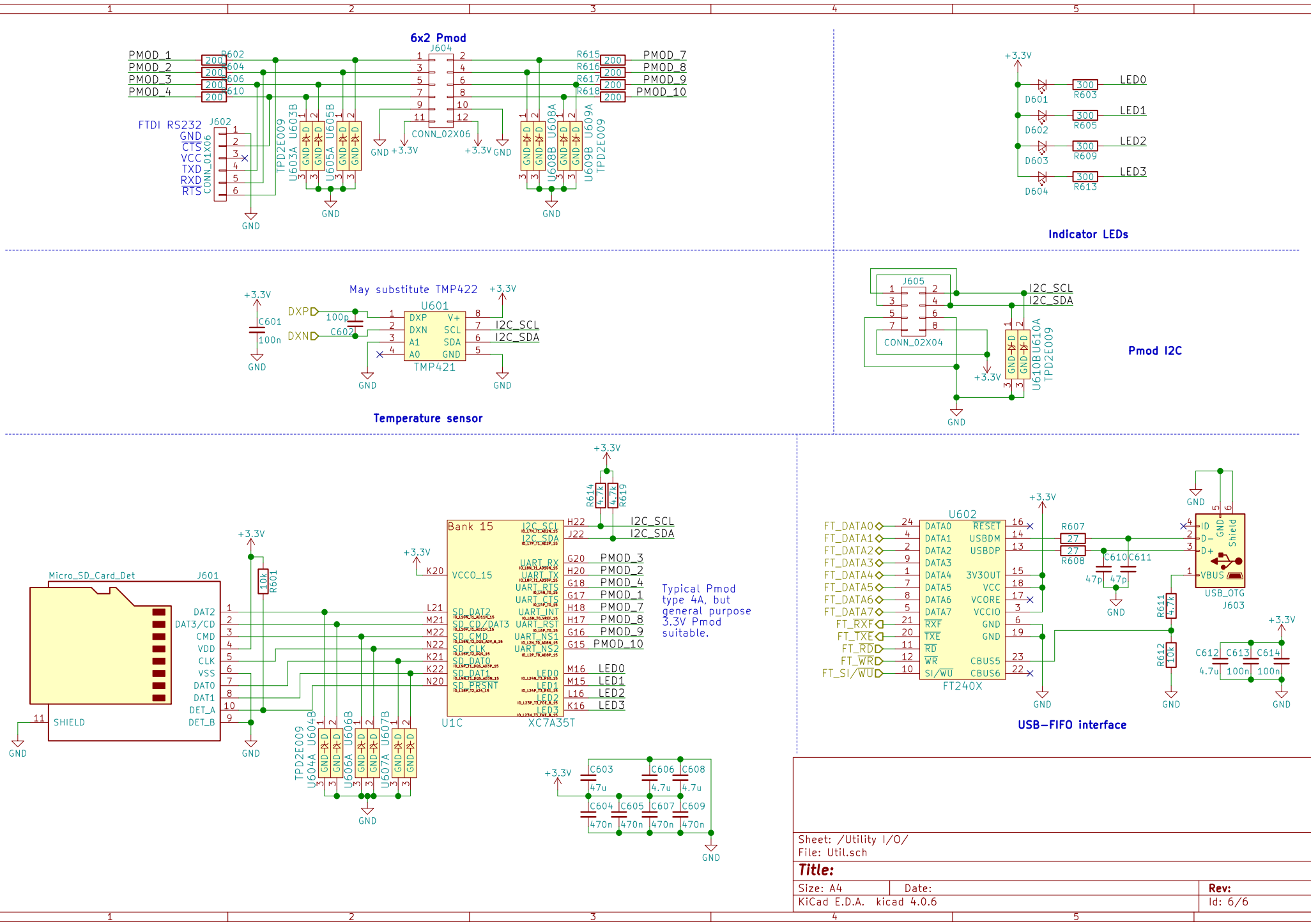
6x2 Pmod
PMOD_1
PMOD_2
PMOD_3
PMOD_4
PMOD_7
PMOD_8
PMOD_9
PMOD_10
FTDI RS232
GND
CTS
VCC
TXD
RXD
RTS
CONN_01X06
CONN_02X06
TPD2E009
Indicator LEDs
LED0
LED1
LED2
LED3
Temperature sensor
May substitute TMP422
TMP421
I2C_SCL
I2C_SDA
Pmod I2C
Micro_SD_Card_Det
SHIELD
Bank 15
VCCO_15
SD_DAT2
SD_CD/DAT3
SD_CMD
SD_CLK
SD_DAT0
SD_DAT1
SD_PRSNT
UART_RX
UART_TX
UART_RTS
UART_CTS
UART_INT
UART_RST
UART_NS1
UART_NS2
XC7A35T
Typical Pmod type 4A, but general purpose 3.3V Pmod suitable.
USB-FIFO interface
FT240X
USB_OTG
Sheet: /Utility I/O/
File: Util.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 4.0.6
Id: 6/6