R61509

262,144-color, 240RGB x 432-dot graphics liquid crystal controller driver supporting MDDI for Amorphous-Silicon TFT Panel

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Description

The R61509 is a single-chip liquid crystal controller driver LSI for a-Si TFT panel, incorporating RAM for a maximum 240 RGB x 432 dot graphics display, source driver, gate driver and power supply circuit. For efficient data transfer, the R61509 supports high-speed interface via 8-/9-/16-/18-bit ports as system interface to the microcomputer and high-speed RAM write function. As moving picture interface, the R61509 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE and DB17-0).

The power supply circuit incorporates step-up circuit and voltage follower circuit to generate TFT liquid crystal panel drive voltages.

The R61509's power management functions such as 8-color display and shut down and so on make this LSI an ideal driver for the medium or small sized portable products with color display systems such as digital cellular phones or small PDAs, where long battery life is a major concern.

Note: The MDDI supported by the R61509 is designed and produced based on the licensing of technology from Qualcomm. The MDDI must be adopted in the module, which incorporates a Qualcomm's CDMA ASIC. Any claims, including, but not limited to the third party's right to use the MDDI for industrial purposes shall not be accepted by Renesas Technology unless the above-mentioned condition is met.

Features

- A single-chip controller driver incorporating a gate circuit and a power supply circuit for a maximum 240RGB x 432dots graphics display on amorphous TFT panel in 262k colors
- System interface
  - High-speed interfaces via 8-, 9-, 16-, 18-bit parallel ports
  - Clock synchronous serial interface
  - Endian free interface, enabling switching endian by software
  - Mobile display system using MDDI (Mobile Display Digital Interface)
    Mobile display system optimized interface
    Sub-display interface compatible with moving picture display
- Moving picture display interface
  - 6-, 16-, 18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  - VSYNC interface (System interface + VSYNC)
  - FMARK interface (System interface + FMARK)
- High-speed RAM write function
- Window address function to specify a rectangular area in the internal RAM to write data
- Write data within a rectangular area in the internal RAM via moving picture interface
  - Reduce data transfer by specifying the area in the RAM to rewrite data
  - Enable displaying the data in the still picture RAM area with a moving picture simultaneously
- Abundant color display and drawing functions
  - Programmable γ-correction function for 262k-color display
  - Partial display function
- Low -power consumption architecture (allowing direct input of interface I/O power supply)
  - Shut down function
  - 8-color display function
  - Input power supply voltages: VCC = 2.5V ~ 3.1 V (logic regulator power supply)
    IOVCC1 = 1.65V ~ 3.1 V (interface I/O power supply)
    IOVCC2 = 2.5V ~ 3.1V (MDDI power supply voltage)
    VCI = 2.5V ~ 3.1 V (liquid crystal analog circuit power supply)
- Incorporates a liquid crystal drive power supply circuit
  - Source driver liquid crystal drive/VCOM power supply: DDVDH-GND = 4.5V ~ 6.0 V
    VCL-GND = -1.9V ~ -3.0V
    VCI-VCL ≤ 6.0V
  - Gate drive power supply: VGH-GND = 10.0V ~ 17.5V
    VGL-GND = -4.5V ~ -12.5V
    VGH-VGL ≤ 28.0V
  - VCOM drive (VCOM power supply): VCOMH = 3.0V ~ (DDVDH-0.5)V
    VCOML = (VCL+0.5)V ~ 0V
    VCOMH-VCOML amplitude = 6.0V (max.)
- Liquid crystal power supply startup sequencer
- TFT storage capacitance: Cst only (common VCOM formula)
- 233,280-byte internal RAM

- Internal 720-channel source driver and 432-channel gate driver
- Single-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate
- Internal NVM

  User identification code: 4 bits
  VCOM level adjustment: 5 bits x 2

Power Supply Specifications

Table 1

No.	Item		R61509
1	TFT data lines		720 output
2	TFT gate lines		432 output
3	TFT display storage capacitance		Cst only (Common VCOM formula)
4	Liquid crystal drive output	S1~S720	V0 ~ V31 grayscales
		G1~G432	VGH-VGL
		VCOM	Change VCOMH-VCOML amplitude with electronic volume Change VCOMH with either electronic volume or from VCOMR
5	Input voltage	IOVCC (interface voltage)	1.65V ~ 3.10V Power supply to IM0/ID, IM1-2, RESET*, DB17-0, RD*, SDI, SDO, WR/SCL, RS, CS*, VSYNC, HSYNC, DOTCLK, ENABLE, FMARK Connect to VCC and VCI on the FPC when the electrical potentials are the same.
		IOVCC2 (MDDI power supply voltage)	2.5V ~ 3.10V
		VCC (logic regulator power supply)	2.50V ~ 3.10V Connect to IOVCC1 and VCI on the FPC when the electrical potentials are the same.
		VCI (liquid crystal drive power supply voltage)	2.50V ~ 3.10V Connect to IOVCC1 and VCC on the FPC when the electrical potentials are the same.
		VPP (NVM power supply)	VPP1: 9.0V ±0.1V
			VPP2: 7.5V ±0.1V
			VPP3A/VPP3B: GND
6	Liquid crystal drive voltages	DDVDH	4.5V ~ 6.0V
		VGH	10.0V ~ 17.5V
		VGL	-4.5V ~ -12.5V
		VGH-VGL	Max. 28.0V
		VCL	-1.9V ~ -3.0V
		VCI-VCL	Max. 6.0V
6	Internal step-up circuits	VLOUT1 (DDVDH)	VCI1 x 2
		VLOUT2 (VGH)	VCI1 x 6, x 7
		VLOUT3 (VGL)	VCI1 x -3, x -4, x -5
		VLOUT4 (VCL)	VCI1 x -1

Block Diagram

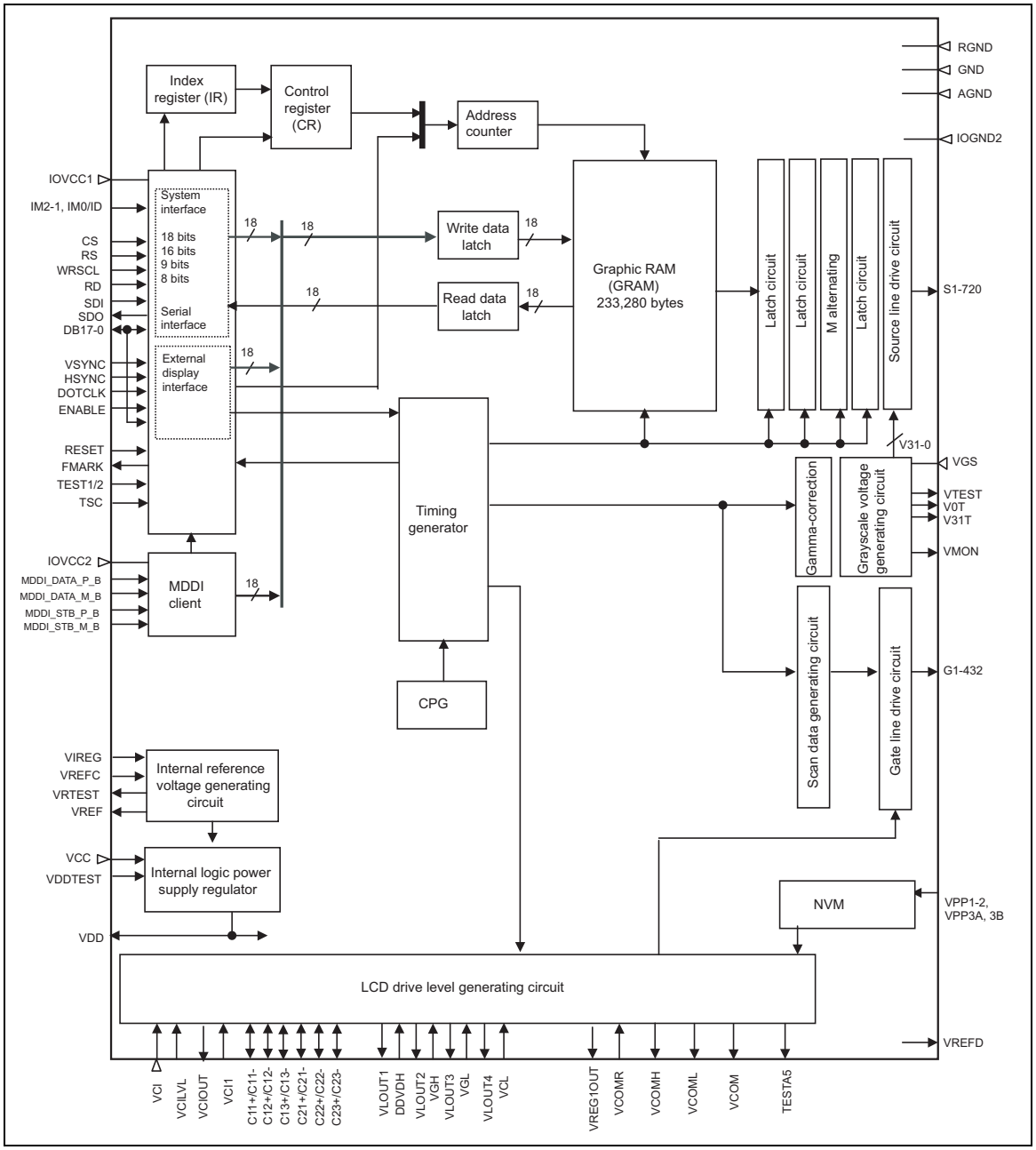


Figure 1

Block Function

1. System Interface

The R61509 supports 80-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and a clock synchronous serial interface. The interface is selected by setting the IM2-0 pins.

The R61509 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control register and internal GRAM. The WDR is the register to temporarily store data to be written to control register and internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the R61509 performs the first read operation from the internal GRAM. Valid data is read out when the R61509 performs the second and subsequent read operation.

The R61509 allows writing instructions consecutively by executing the instruction in the same cycle when it is written (0 instruction cycle).

Table 2 Register Selection (80-System 8/9/16/18-Bit Parallel Interface)

WR*	RD*	RS	Function
0	1	0	Write index to IR
1	0	0	Setting disabled
0	1	1	Write to control register or internal GRAM via WDR
1	0	1	Read from internal GRAM and register via RDR

Table 3 Register Selection (Clock Synchronous Serial Interface)

Start byte		
R/W	RS	Function
0	0	Write index to IR
1	0	Setting disabled
0	1	Write to control register or internal GRAM via WDR
1	1	Read from internal GRAM and register via RDR

Table 4

IM2	IM1	IM0	System interface	DB pins	RAM write data	Instruction write transfer
0	0	0	80-system 18-bit interface	DB17-0	Single transfer (18 bits)	Single transfer (16 bits)
0	0	1	80-system 9-bit interface	DB17-9	2-transfer (1^{st}: 9 bits, 2^{nd}: 9 bits)	2-transfer (1^{st}: 8 bits, 2^{nd}: 8 bits)
0	1	0	80-system 16-bit interface	DB17-10, DB8-1	Single transfer (16 bits) 2-transfer (1^{st}: 2 bits, 2^{nd}: 16 bits) 2-transfer (1^{st}: 16 bits, 2^{nd}: 2 bits)	Single transfer (16 bits)
0	1	1	80-system 8-bit interface	DB17-10	2-transfer (1^{st}: 8 bits, 2^{nd}: 8 bits) 3-transfer (1^{st}: 2 bits, 2^{nd}: 8 bits, 3^{rd}: 8 bits) 3-transfer (1^{st}: 6 bits, 2^{nd}: 6 bits, 3^{rd}: 6 bits)	2-transfer (1^{st}: 8 bits, 2^{nd}: 8 bits)
1	0	*	Clock synchronous serial interface	- (SDI, SDO)	2-transfer (1^{st}: 8 bits, 2^{nd}: 8 bits)	2-transfer (1^{st}: 8 bits, 2^{nd}: 8 bits)
1	1	0	Setting disabled	-	-	-
1	1	1	MDDI	(MDDI_STB_P/M_B, MDDI_DATA_P/M_B)	16 bpp, 18 bpp	-

2. External Display Interface (RGB, VSYNC interfaces)

The R61509 supports RGB interface and VSYNC interface as the external interface to display moving picture. When the RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB17-0) is written in synchronization with these signals when the polarity of enable signal (ENABLE) allows write operation in order to prevent flicker while updating display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, which synchronizes the display operation with the VSYNC signal. The display data is written to the internal GRAM via system interface. When writing data via VSYNC interface, there are constraints in speed and method in writing data to the internal RAM. For details, see the "VSYNC interface" section.

The R61509 allows switching interface by instruction according to the display, i.e. still and/or moving picture(s) in order to transfer data only when the data is updated and thereby reduce the data transfer and power consumption for moving picture display.

3. MDDI (Mobile Display Digital Interface)

The R61509 supports a MDDI client as a differential small-amplitude high-speed direct interface to the MDDI host via MDDI_STB_P_B, MDDI_STB_M, MDDI_DATA_P_B, and MDDI_DATA_M_B.

The MDDI or system interface is selected by setting IM2-0 pins.

The MDDI circuit supported by the R61509 is compliant with the MDDI specifications disclosed in VESA (Video Electronics Standards Association). The R61509 enables an easy configuration of cost-effective differential interface mobile display system by optimizing the MDDI specifications to the mobile display.

4. Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register to set a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As the R61509 writes data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only within the rectangular area specified in the GRAM.

5. Graphics RAM (GRAM)

GRAM stands for graphics RAM, which can store bit-pattern data of 233,280 (240RGB x 432 (dots) x 18(bits)) bytes at maximum, using 18 bits per pixel.

6. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltages according to the grayscale data in the γ-correction registers to enable 262k-color display. For details, see the γ-Correction Register section.

7. Liquid Crystal Drive Power Supply Circuit

The liquid crystal drive power supply circuit generates DDVDH, VGH, VGL and VCOM levels to drive liquid crystal.

8. Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal GRAM. The timing signal for display operation such as RAM read operation and the timing signal for internal operation such as RAM access from the MPU are generated separately in order to avoid mutual interference.

9. Oscillator (OSC)

The R61509 generates the RC oscillation clock internally. Connecting an external oscillation resistor between the OSC1 and OSC2 pins to generate the clock is not possible. The oscillation frequency is set to 678 kHz before shipment (for details, see Electrical Characteristics). Set the frame frequency adjustment function to change the number of display lines and the frame frequency. While the R61509 is shut down, RC oscillation halts so that reduce power consumption is reduced.

10. Liquid crystal driver Circuit

The liquid crystal driver circuit of the R61509 consists of a 720-output source driver (S1 ~ S720) and a 432-output gate driver (G1~G432). The display pattern data is latched when 240RGB of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate

lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the SS bit and the shift direction of gate output from the gate driver can be changed by setting the GS bit. The scan mode by the gate driver can be changed by setting the SM bit.

11. Internal Logic Power Supply Regulator

The internal logic power supply regulator generates internal logic power supply VDD.

Pin Function

Table 5 Interface Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>IM2-1, IM0/ID</td><td>I</td><td>GND or IOVCC1</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code. Amplitude: IOVCC1-GND
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 see Note 1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 see Note 2</td></tr>
<tr><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>65,536</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>MDDI</td><td>MDDI_DATA_P/M_B, MDDI_DATA_P\M_B</td><td>262,144 see note 3</td></tr>
</table>
Notes: 1. 65,536 colors in one transfer mode.
2. 65,536 colors in two transfers mode.
3. 65,536 colors in MDDI operation (DFM = 1).</td><td>-</td></tr>
<tr><td>CS*</td><td>I</td><td>MPU</td><td>Chip select signal. Amplitude: IOVCC1-GND
Low: the R61509 is selected and accessible
High: the R61509 is not selected and not accessible.</td><td>IOVCC1</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal. Amplitude: IOVCC1-GND
Low: select Index or status register
High: select control register</td><td>IOVCC1</td></tr>
<tr><td>WR*/SCL</td><td>I</td><td>MPU</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when WR* is low. Synchronous clock signal (SCL) in serial interface operation. Amplitude: IOVCC1-GND</td><td>IOVCC1</td></tr>
<tr><td>RD*</td><td>I</td><td>MPU</td><td>Read strobe signal in 80-system bus interface operation and enables read operation when RD* is low. Amplitude: IOVCC1-GND</td><td>IOVCC1</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>Serial data input (SDI) pin in serial interface operation. The data is inputted on the rising edge of the SCL signal. Amplitude: IOVCC1-GND</td><td>GND or IOVCC1</td></tr>
<tr><td rowspan="2">SDO</td><td rowspan="2">O</td><td>MPU</td><td>Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. Amplitude: IOVCC1-GND</td><td rowspan="2">Open (MDDDI: open)</td></tr>
<tr><td>Peripheral control</td><td>In MDDI operation, SDO is assigned for the sub-display interface output (CS).</td></tr>
</table>

Signal	I/O	Connect to	Function	When not in use
DB0-DB17	I/O	MPU	18-bit parallel bi-directional data bus for 80-system interface operation (Amplitude: IOVCC1-GND). 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-1 are used. 18-bit I/F: DB17-DB0 are used. 18-bit parallel bi-directional data bus for RGB interface operation (Amplitude: IOVCC1-GND). 6-bit I/F: DB17-DB12 are used. 16-bit I/F: DB17-DB13 and DB11-1 are used. 18-bit I/F: DB17-DB0 are used. Sub-display interface output for MDDI. Sub-display I/F: DB 17-0	GND or IOVCC1 (MDDI: Open)
ENABLE	I	MPU	Data enable signal for RGB interface operation. (Amplitude: IOVCC1-GND). Low: accessible (select) High: Not accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit (Amplitude: IOVCC1-GND).	GND or IOVCC1 (MDDI: open)
	O	Peripheral control	In MDDI operation, ENABLE is assigned for the sub-display interface output (WR).	
VSYNC	I	MPU	Frame synchronous signal for RGB interface operation. Low active. (Amplitude: IOVCC1-GND).	GND or IOVCC1
HSYNC	I	MPU	Line synchronous signal for RGB interface operation. Low active. (Amplitude: IOVCC1-GND).	GND or IOVCC1
	O	Peripheral control	In MDDI operation, HSYNC is assigned for the sub-display interface output (RS).	(MDDI: open)
DOTCLK	I	MPU	Dot clock signal for RGB interface operation. The data input timing is on the rising edge of DOTCLK. (Amplitude: IOVCC1-GND).	GND or IOVCC1
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM. (Amplitude: IOVCC1-GND).	Open
TSC	I	Sub display	Sub display FLM signal, which is input from TSC pin when FMKM = 1 (Amplitude: IOVCC1-GND).	GND

Table 6 MDDI (Mobile Display Digital Interface)

Signal	Pin No.	I/O	Connect to	Function	When not in use
MDDI_DATA_P_B, MDDI_DATA_M_B	One each	I	MDDI host	MDDI data signal lines. Data+ (MDDI_DATA_P_B) and Data- (MDDI_DATA_M_B) are differential small-amplitude signals. Make the wiring as short as possible so that the COG resistance becomes less than 10 ohm. The specifications of interface must be compliant with the MDDI specifications.	Open
MDDI_STB_P_B, MDDI_STB_M_B	One each	I	MDDI host	MDDI strobe signal lines. Stb+ (MDDI_STB_P_B) and Stb- (MDDI_STB_M_B) are differential small-amplitude signals. Make the wiring as short as possible so that the COG resistance becomes less than 10 ohm. The specifications of interface must be compliant with the MDDI specifications.	Open

Table 7 Reset Pin

Signal	Pin No.	I/O	Connect to	Function	When not in use
RESET*	1	I	MPU or external RC circuit	Reset signal. Initializes the R61509 when it is low. Make sure to execute a power-on reset when turning on power supply (IOVCC1-GND amplitude signal).	-

Table 8 Power Supply Pins

Signal	Pin No.	I/O	Connect to	Function	When not in use
VCC	1	-	Power supply	Power supply to internal logic regulator circuit: VCC = 2.5V~3.1V. VCC ≥ IOVCC1, IOVCC2.	-
GND	1	-	Power supply	GND for internal logic and interface pins (RESET, CS, WR, RD, RS, DB15-0, VSYNC, HSYNC, DOTCLK and ENABLE). GND = 0V.	-
RGND	1	-	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.	-
VDD VDDOUT	One each	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.	-
IOVCC1	1	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC1 = 1.65V ~ 3.1V. VCC ≥ IOVCC1. In case of COG, connect to VCC on the FPC to prevent noise when VCC = IOVCC1 = IOVCC2.	-
IOVCC2	1	-	Power supply	Power supply to the MDDI pins, MDDI_DATA_P_B, MDDI_DATA_M_B, MDDI_STB_P_B, and MDDI_STB_M_B (IOVCC2 = 2.5V ~ 3.1V, VCC ≥ IOVCC2). Connect to power supply when MDDI is not used. In case of COG, connect to VCC on the FPC when VCC = IOVCC1 = IOVCC2.	
IOGND2	1	-	Power supply	Power supply to the MDDI pins, MDDI_DATA_P_B, MDDI_DATA_M_B, MDDI_STB_P_B, and MDDI_STB_M_B (IOGND2 = 0V). Connect to GND when MDDI is not used. In case of COG, connect to GND on the FPC to prevent noise.	
AGND	1	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.	-
VCI	1	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.1V.	-
VCILVL	1	I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.1V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.	-
VIREG	1	I	External resistor	Reference power supply pin for MDDI. Connect a resistor of 220kΩ (≤ ±1%) between VIREG and GND. When connecting the resistor, 1. Make the wiring from the IC as short as possible. 2. Shield the VIREG wiring (including those on glass substrate) and connect the shield to GND. 3. Make sure other wiring is not laid over or underneath the VIREG wiring.	IOGND2
VPP1	1	I	Power supply	Internal NVM power supply. Apply the following voltages on VPP1 ~ VPP2 respectively according to the power supply ON sequence.	Open
VPP2	1	I	Power supply	**Operation mode** / **VPP1** / **VPP2** / **VPP3A, 3B** NVM write / 9.0±0.1V / 7.5±0.1V / GND NVM read / Open / Open / GND	Open
VPP3A, 3B	One each	I	Power supply		GND

Table 9 Step-Up Circuit

Signal	I/O	Connect to	Function	When not in use
VCIOUT	O	Stabilizing capacitor, VCI1	Output voltage from the step-up circuit 1, generated from the reference voltage. VC bits set the output factor.	
VCI1	I/O	VCIOUT	Reference voltage of step-up circuit 1. Make sure the output voltage levels from VLOUT1, VLOUT2, VLOUT3 and VLOUT4 do not exceed the respective setting ranges.	-
VLOUT1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1, generated from VCI1. The step-up factor is set by instruction (BT bits). VLOUT1 = 4.5V ~ 6.0V	-
DDVDH	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and VCOM drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V	-
VLOUT2	O	Stabilizing capacitor, VGH	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by instruction (BT bits). VLOUT2 = max 17.5V	-
VGH	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.	-
VLOUT3	O	Stabilizing capacitor, VGL	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by instruction (BT bits). VLOUT3 = min –12.5V	-
VGL	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.	-
VLOUT4	O	Stabilizing capacitor, VCL	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by instruction (BT bits). VLOUT4 = -1.9V ~ -3.0V	-
VCL	O	Stabilizing capacitor	VCOML drive power supply. Connect to VLOUT4. Capacitor connection is not required when VCOMG = 0 (VCOML = GND). VCL = GND.	-
C11+, C11- C12+, C12-	I O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.	-
C13+, C13- C21+, C21- C22+, C22- C23+, C23-	I O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.	-

Table 10 LCD drive

Signal	I/O	Connect to	Function	When not in use
VREG1OUT	O	Stabilizing capacitor	Output voltage generated from the reference voltage either VCILVL voltage (inputted from outside) or VCIR voltage (internally generated). The factor is determined by instruction (VRH bits). VREG1OUT is used for (1) source driver grayscale reference voltage VDH, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Connect to a stabilizing capacitor when in use. VREG1OUT =4.0V ~ (DDVDH – 0.5)V	Open
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.	Open
VCOMH	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by either external resistor (VCOMR) or electronic volume.	Open
VCOML	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). VCOML = (VCL+0.5) V ~ 0V	Open
VCOMR	I	Variable resistor or open	Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND.	Open
VGS	I	GND	Reference level for the grayscale voltage generating circuit.	-
S1~S720	O	LCD	Liquid crystal application voltages. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is outputted from S1. When SS = 1, the data in the RAM address h00000 is outputted from S720.	Open
G1~G432	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level	Open

Table 11 Others (test, dummy pins)

Signal	I/O	Connect to	Function	When not in use
V0T, V31T	I/O	Open	Test pins. Leave open.	Open
VTEST	O	Open	Test pin. Leave open.	Open
VREFC	I	AGND	Test pin. Make sure to fix to the AGND level.	-
VREF	O	Open	Test pin. Leave open.	Open
VDDTEST	I	AGND	Test pin. Make sure to fix to the AGND level.	-
VREFD	O	Open	Test pin. Leave open.	Open
VMON	O	Open	Test pin. Leave open.	Open
TESTA5	O	Open	Test pin. Leave open.	Open
IOVCCDUM1-2	O	-	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave open.	Open
VCCDUM1	O	-	Test pin. Leave open	Open
GNDDUM1-21	O	-	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave open.	Open
IOGND2DUM1-8	O	-	Dummy pins between MDDI pins. Leave open.	Open
AGNDDUM1-5	O	-	Use them to fix VREFC, VDDTEST.	Open
DUMMYR 1-10	-	-	DUMMYR1 and DUMMYR10, DUMMYR2 and DUMMYR9, DUMMYR3 and DUMMYR4, DUMMYR5 and DUMMYR8, and DUMMYR6 and DUMMYR7 are short-circuited within the chip for COG contact resistance measurement.	Open
VGLDMY 1-4	O	-	Dummy pads. Leave them open.	Open
TESTO1-18	O	-	Dummy pads. Leave them open.	Open
TEST1-3	I	GND	Test pins. Connect to GND.	GND

Patents of dummy pin which is used to fix pin to VCC or GND are pending or granted.

PATENT ISSUED: United States Patent No. 6,323,930
PATENT PENDING: Japanese Application No. 10-514484, Korean Application No. 19997002322
Taiwanese Application No.086103756, (PCT/JP96/02728(W098/12597)

■R61509 Pad Arrangement

2006.05.18

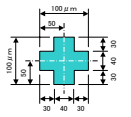
R61509
- ●Chip size: 21.55 x 1.44mm (31.03mm2)
- ●Chip thickness: 280 μm
- ●Pad coordinate: Pad center
- ●Coordinate origin: Chip center

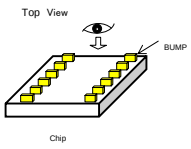
●Au bump size:
(1)50.00 μm × 80.00 μm
No.1 ~ 299
(Pad pitch 70 μm)

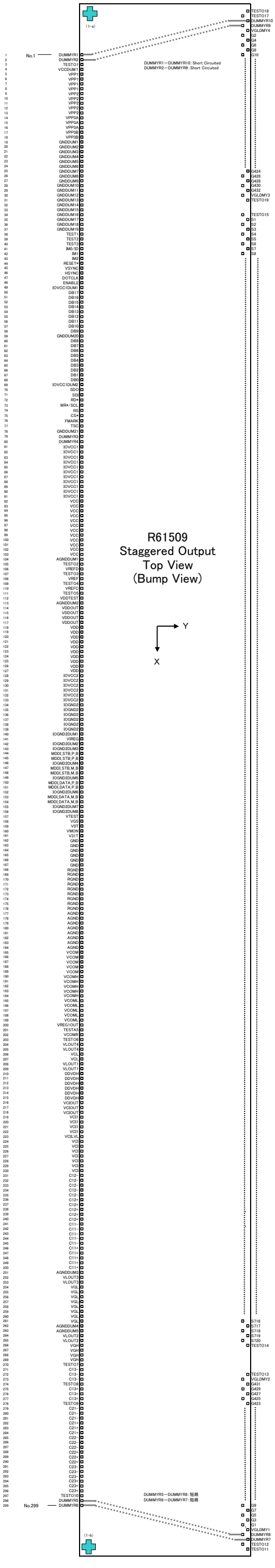
(2)18.00 μm × 110.00 μm
No.300 ~ 1467
(Pad pitch: staggered, 18 μm)

- ●Au bump pitch: See pad coordinate
- ●Au bump height: 15 μm(typ.)
- ●Numbers on figures contained in this data sheet are pad coordinate number.

●Alignment Mark
(1-a), (1-b)







●Chip size: 21.55mm×1.44mm
●Chip thickness: 280μm
●Pad coordinates: Pad center
●Coordinate origin: Chip center

●Au bump size
1. 50μm x 80μm (I/O side: No.1-299)
2. 18μm x 110μm (LCD output side: No.300-1467)

●Au bump pitch: Refer to pad coordinate

●Au bump height:15μm
Note: Numbers on figures contained in this data sheet are pad coordinate number.

●Alignment mark

Alignment marks	X-axis	Y-axis
Type A	-10608.0	-548.0
	10608.0	-548.0

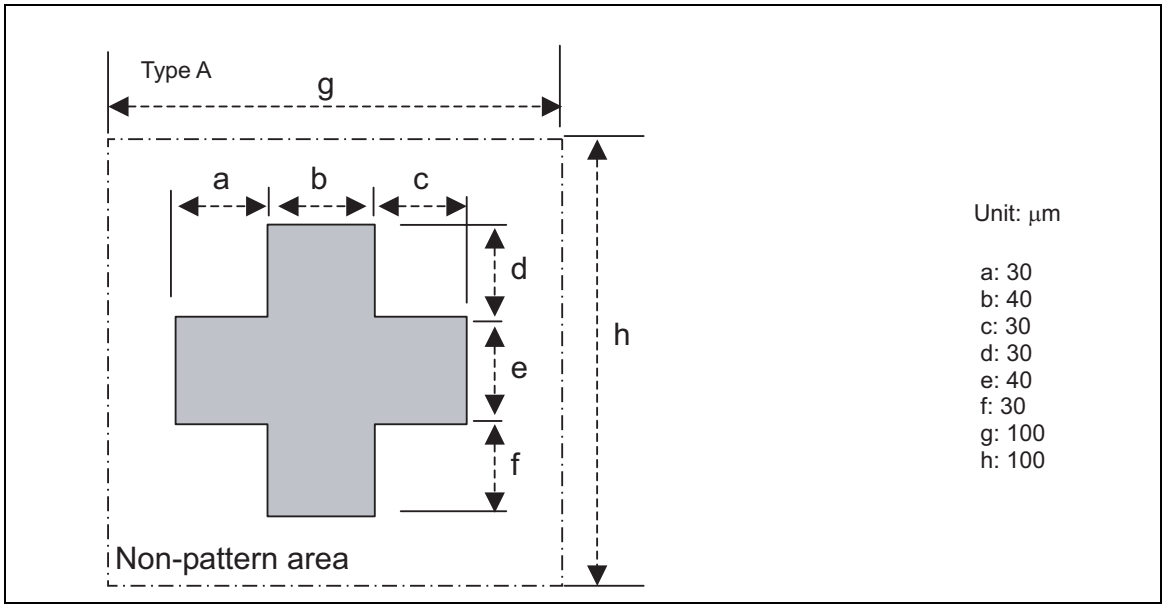


Figure 2

R61509 Pad Coordinate（Unit:μm）

2006.05.18 rev.1.0.1

pad No	pad name	X	Y
1	DUMMYR1	-10430.0	-597.5
2	DUMMYR2	-10360.0	-597.5
3	TESTO1	-10290.0	-597.5
4	VCCDUM1	-10220.0	-597.5
5	VPP1	-10150.0	-597.5
6	VPP1	-10080.0	-597.5
7	VPP1	-10010.0	-597.5
8	VPP1	-9940.0	-597.5
9	VPP2	-9870.0	-597.5
10	VPP2	-9800.0	-597.5
11	VPP2	-9730.0	-597.5
12	VPP2	-9660.0	-597.5
13	VPP2	-9590.0	-597.5
14	VPP3A	-9520.0	-597.5
15	VPP3A	-9450.0	-597.5
16	VPP3A	-9380.0	-597.5
17	VPP3B	-9310.0	-597.5
18	VPP3B	-9240.0	-597.5
19	GNDDUM1	-9170.0	-597.5
20	GNDDUM2	-9100.0	-597.5
21	GNDDUM3	-9030.0	-597.5
22	GNDDUM4	-8960.0	-597.5
23	GNDDUM5	-8890.0	-597.5
24	GNDDUM6	-8820.0	-597.5
25	GNDDUM7	-8750.0	-597.5
26	GNDDUM8	-8680.0	-597.5
27	GNDDUM9	-8610.0	-597.5
28	GNDDUM10	-8540.0	-597.5
29	GNDDUM11	-8470.0	-597.5
30	GNDDUM12	-8400.0	-597.5
31	GNDDUM13	-8330.0	-597.5
32	GNDDUM14	-8260.0	-597.5
33	GNDDUM15	-8190.0	-597.5
34	GNDDUM16	-8120.0	-597.5
35	GNDDUM17	-8050.0	-597.5
36	GNDDUM18	-7980.0	-597.5
37	GNDDUM19	-7910.0	-597.5
38	TEST1	-7840.0	-597.5
39	TEST2	-7770.0	-597.5
40	TEST3	-7700.0	-597.5
41	IM0/ID	-7630.0	-597.5
42	IM1	-7560.0	-597.5
43	IM2	-7490.0	-597.5
44	RESET*	-7420.0	-597.5
45	VSYNC	-7350.0	-597.5
46	HSYNC	-7280.0	-597.5
47	DOTCLK	-7210.0	-597.5
48	ENABLE	-7140.0	-597.5
49	IOVCC1DUM1	-7070.0	-597.5
50	DB17	-7000.0	-597.5

pad No	pad name	X	Y
51	DB16	-6930.0	-597.5
52	DB15	-6860.0	-597.5
53	DB14	-6790.0	-597.5
54	DB13	-6720.0	-597.5
55	DB12	-6650.0	-597.5
56	DB11	-6580.0	-597.5
57	DB10	-6510.0	-597.5
58	DB9	-6440.0	-597.5
59	GNDDUM20	-6370.0	-597.5
60	DB8	-6300.0	-597.5
61	DB7	-6230.0	-597.5
62	DB6	-6160.0	-597.5
63	DB5	-6090.0	-597.5
64	DB4	-6020.0	-597.5
65	DB3	-5950.0	-597.5
66	DB2	-5880.0	-597.5
67	DB1	-5810.0	-597.5
68	DB0	-5740.0	-597.5
69	IOVCC1DUM2	-5670.0	-597.5
70	SDO	-5600.0	-597.5
71	SDI	-5530.0	-597.5
72	RD*	-5460.0	-597.5
73	WR*/SCL	-5390.0	-597.5
74	RS	-5320.0	-597.5
75	CS*	-5250.0	-597.5
76	FMARK	-5180.0	-597.5
77	TSC	-5110.0	-597.5
78	GNDDUM21	-5040.0	-597.5
79	DUMMYR3	-4970.0	-597.5
80	DUMMYR4	-4900.0	-597.5
81	IOVCC1	-4830.0	-597.5
82	IOVCC1	-4760.0	-597.5
83	IOVCC1	-4690.0	-597.5
84	IOVCC1	-4620.0	-597.5
85	IOVCC1	-4550.0	-597.5
86	IOVCC1	-4480.0	-597.5
87	IOVCC1	-4410.0	-597.5
88	IOVCC1	-4340.0	-597.5
89	IOVCC1	-4270.0	-597.5
90	IOVCC1	-4200.0	-597.5
91	IOVCC1	-4130.0	-597.5
92	VCC	-4060.0	-597.5
93	VCC	-3990.0	-597.5
94	VCC	-3920.0	-597.5
95	VCC	-3850.0	-597.5
96	VCC	-3780.0	-597.5
97	VCC	-3710.0	-597.5
98	VCC	-3640.0	-597.5
99	VCC	-3570.0	-597.5
100	VCC	-3500.0	-597.5

R61509 Pad Coordinate（Unit:μm）

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pad No	pad name	X	Y
101	VCC	-3430.0	-597.5
102	VCC	-3360.0	-597.5
103	VCC	-3290.0	-597.5
104	AGNDDUM1	-3220.0	-597.5
105	TESTO2	-3150.0	-597.5
106	VREFD	-3080.0	-597.5
107	TESTO3	-3010.0	-597.5
108	VREF	-2940.0	-597.5
109	TESTO4	-2870.0	-597.5
110	VREFC	-2800.0	-597.5
111	TESTO5	-2730.0	-597.5
112	VDDTEST	-2660.0	-597.5
113	AGNDDUM2	-2590.0	-597.5
114	VDDOUT	-2520.0	-597.5
115	VDDOUT	-2450.0	-597.5
116	VDDOUT	-2380.0	-597.5
117	VDDOUT	-2310.0	-597.5
118	VDD	-2240.0	-597.5
119	VDD	-2170.0	-597.5
120	VDD	-2100.0	-597.5
121	VDD	-2030.0	-597.5
122	VDD	-1960.0	-597.5
123	VDD	-1890.0	-597.5
124	VDD	-1820.0	-597.5
125	VDD	-1750.0	-597.5
126	VDD	-1680.0	-597.5
127	VDD	-1610.0	-597.5
128	IOVCC2	-1540.0	-597.5
129	IOVCC2	-1470.0	-597.5
130	IOVCC2	-1400.0	-597.5
131	IOVCC2	-1330.0	-597.5
132	IOVCC2	-1260.0	-597.5
133	IOVCC2	-1190.0	-597.5
134	IOGND2	-1120.0	-597.5
135	IOGND2	-1050.0	-597.5
136	IOGND2	-980.0	-597.5
137	IOGND2	-910.0	-597.5
138	IOGND2	-840.0	-597.5
139	IOGND2	-770.0	-597.5
140	IOGND2DUM1	-700.0	-597.5
141	VIREG	-630.0	-597.5
142	IOGND2DUM2	-560.0	-597.5
143	IOGND2DUM3	-490.0	-597.5
144	MDDI_STB_P_B	-420.0	-597.5
145	MDDI_STB_P_B	-350.0	-597.5
146	IOGND2DUM4	-280.0	-597.5
147	MDDI_STB_M_B	-210.0	-597.5
148	MDDI_STB_M_B	-140.0	-597.5
149	IOGND2DUM5	-70.0	-597.5
150	MDDI_DATA_P_B	0.0	-597.5

pad No	pad name	X	Y
151	MDDI_DATA_P_B	70.0	-597.5
152	IOGND2DUM6	140.0	-597.5
153	MDDI_DATA_M_B	210.0	-597.5
154	MDDI_DATA_M_B	280.0	-597.5
155	IOGND2DUM7	350.0	-597.5
156	IOGND2DUM8	420.0	-597.5
157	VTEST	490.0	-597.5
158	VGS	560.0	-597.5
159	V0T	630.0	-597.5
160	VMON	700.0	-597.5
161	V31T	770.0	-597.5
162	GND	840.0	-597.5
163	GND	910.0	-597.5
164	GND	980.0	-597.5
165	GND	1050.0	-597.5
166	GND	1120.0	-597.5
167	GND	1190.0	-597.5
168	RGND	1260.0	-597.5
169	RGND	1330.0	-597.5
170	RGND	1400.0	-597.5
171	RGND	1470.0	-597.5
172	RGND	1540.0	-597.5
173	RGND	1610.0	-597.5
174	RGND	1680.0	-597.5
175	RGND	1750.0	-597.5
176	RGND	1820.0	-597.5
177	AGND	1890.0	-597.5
178	AGND	1960.0	-597.5
179	AGND	2030.0	-597.5
180	AGND	2100.0	-597.5
181	AGND	2170.0	-597.5
182	AGND	2240.0	-597.5
183	AGND	2310.0	-597.5
184	AGND	2380.0	-597.5
185	VCOM	2450.0	-597.5
186	VCOM	2520.0	-597.5
187	VCOM	2590.0	-597.5
188	VCOM	2660.0	-597.5
189	VCOM	2730.0	-597.5
190	VCOMH	2800.0	-597.5
191	VCOMH	2870.0	-597.5
192	VCOMH	2940.0	-597.5
193	VCOMH	3010.0	-597.5
194	VCOMH	3080.0	-597.5
195	VCOML	3150.0	-597.5
196	VCOML	3220.0	-597.5
197	VCOML	3290.0	-597.5
198	VCOML	3360.0	-597.5
199	VCOML	3430.0	-597.5
200	VREG1OUT	3500.0	-597.5

R61509 Pad Coordinate（Unit:μm）

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pad No	pad name	X	Y
201	TESTA5	3570.0	-597.5
202	VCOMR	3640.0	-597.5
203	TESTO6	3710.0	-597.5
204	VLOUT4	3780.0	-597.5
205	VLOUT4	3850.0	-597.5
206	VCL	3920.0	-597.5
207	VCL	3990.0	-597.5
208	VLOUT1	4060.0	-597.5
209	VLOUT1	4130.0	-597.5
210	DDVDH	4200.0	-597.5
211	DDVDH	4270.0	-597.5
212	DDVDH	4340.0	-597.5
213	DDVDH	4410.0	-597.5
214	DDVDH	4480.0	-597.5
215	DDVDH	4550.0	-597.5
216	VCIOUT	4620.0	-597.5
217	VCIOUT	4690.0	-597.5
218	VCIOUT	4760.0	-597.5
219	VCI1	4830.0	-597.5
220	VCI1	4900.0	-597.5
221	VCI1	4970.0	-597.5
222	VCI1	5040.0	-597.5
223	VCILVL	5110.0	-597.5
224	VCI	5180.0	-597.5
225	VCI	5250.0	-597.5
226	VCI	5320.0	-597.5
227	VCI	5390.0	-597.5
228	VCI	5460.0	-597.5
229	VCI	5530.0	-597.5
230	VCI	5600.0	-597.5
231	C12-	5670.0	-597.5
232	C12-	5740.0	-597.5
233	C12-	5810.0	-597.5
234	C12-	5880.0	-597.5
235	C12-	5950.0	-597.5
236	C12+	6020.0	-597.5
237	C12+	6090.0	-597.5
238	C12+	6160.0	-597.5
239	C12+	6230.0	-597.5
240	C12+	6300.0	-597.5
241	C11-	6370.0	-597.5
242	C11-	6440.0	-597.5
243	C11-	6510.0	-597.5
244	C11-	6580.0	-597.5
245	C11-	6650.0	-597.5
246	C11+	6720.0	-597.5
247	C11+	6790.0	-597.5
248	C11+	6860.0	-597.5
249	C11+	6930.0	-597.5
250	C11+	7000.0	-597.5

pad No	pad name	X	Y
251	AGNDDUM3	7070.0	-597.5
252	VLOUT3	7140.0	-597.5
253	VLOUT3	7210.0	-597.5
254	VGL	7280.0	-597.5
255	VGL	7350.0	-597.5
256	VGL	7420.0	-597.5
257	VGL	7490.0	-597.5
258	VGL	7560.0	-597.5
259	VGL	7630.0	-597.5
260	VGL	7700.0	-597.5
261	VGL	7770.0	-597.5
262	AGNDDUM4	7840.0	-597.5
263	AGNDDUM5	7910.0	-597.5
264	VLOUT2	7980.0	-597.5
265	VLOUT2	8050.0	-597.5
266	VGH	8120.0	-597.5
267	VGH	8190.0	-597.5
268	VGH	8260.0	-597.5
269	VGH	8330.0	-597.5
270	TESTO7	8400.0	-597.5
271	C13-	8470.0	-597.5
272	C13-	8540.0	-597.5
273	C13-	8610.0	-597.5
274	TESTO8	8680.0	-597.5
275	C13+	8750.0	-597.5
276	C13+	8820.0	-597.5
277	C13+	8890.0	-597.5
278	TESTO9	8960.0	-597.5
279	C21-	9030.0	-597.5
280	C21-	9100.0	-597.5
281	C21-	9170.0	-597.5
282	C21+	9240.0	-597.5
283	C21+	9310.0	-597.5
284	C21+	9380.0	-597.5
285	C22-	9450.0	-597.5
286	C22-	9520.0	-597.5
287	C22-	9590.0	-597.5
288	C22+	9660.0	-597.5
289	C22+	9730.0	-597.5
290	C22+	9800.0	-597.5
291	C23-	9870.0	-597.5
292	C23-	9940.0	-597.5
293	C23-	10010.0	-597.5
294	C23+	10080.0	-597.5
295	C23+	10150.0	-597.5
296	C23+	10220.0	-597.5
297	TESTO10	10290.0	-597.5
298	DUMMYR5	10360.0	-597.5
299	DUMMYR6	10430.0	-597.5
300	TESTO11	10647.0	602.0

R61509 Pad Coordinate（Unit:μm）

2006.05.16 rev.1.0

pad No	pad name	X	Y
301	TESTO12	10629.0	467.0
302	DUMMYR7	10611.0	602.0
303	DUMMYR8	10593.0	467.0
304	VGLDMY1	10575.0	602.0
305	G1	10557.0	467.0
306	G3	10539.0	602.0
307	G5	10521.0	467.0
308	G7	10503.0	602.0
309	G9	10485.0	467.0
310	G11	10467.0	602.0
311	G13	10449.0	467.0
312	G15	10431.0	602.0
313	G17	10413.0	467.0
314	G19	10395.0	602.0
315	G21	10377.0	467.0
316	G23	10359.0	602.0
317	G25	10341.0	467.0
318	G27	10323.0	602.0
319	G29	10305.0	467.0
320	G31	10287.0	602.0
321	G33	10269.0	467.0
322	G35	10251.0	602.0
323	G37	10233.0	467.0
324	G39	10215.0	602.0
325	G41	10197.0	467.0
326	G43	10179.0	602.0
327	G45	10161.0	467.0
328	G47	10143.0	602.0
329	G49	10125.0	467.0
330	G51	10107.0	602.0
331	G53	10089.0	467.0
332	G55	10071.0	602.0
333	G57	10053.0	467.0
334	G59	10035.0	602.0
335	G61	10017.0	467.0
336	G63	9999.0	602.0
337	G65	9981.0	467.0
338	G67	9963.0	602.0
339	G69	9945.0	467.0
340	G71	9927.0	602.0
341	G73	9909.0	467.0
342	G75	9891.0	602.0
343	G77	9873.0	467.0
344	G79	9855.0	602.0
345	G81	9837.0	467.0
346	G83	9819.0	602.0
347	G85	9801.0	467.0
348	G87	9783.0	602.0
349	G89	9765.0	467.0
350	G91	9747.0	602.0

pad No	pad name	X	Y
351	G93	9729.0	467.0
352	G95	9711.0	602.0
353	G97	9693.0	467.0
354	G99	9675.0	602.0
355	G101	9657.0	467.0
356	G103	9639.0	602.0
357	G105	9621.0	467.0
358	G107	9603.0	602.0
359	G109	9585.0	467.0
360	G111	9567.0	602.0
361	G113	9549.0	467.0
362	G115	9531.0	602.0
363	G117	9513.0	467.0
364	G119	9495.0	602.0
365	G121	9477.0	467.0
366	G123	9459.0	602.0
367	G125	9441.0	467.0
368	G127	9423.0	602.0
369	G129	9405.0	467.0
370	G131	9387.0	602.0
371	G133	9369.0	467.0
372	G135	9351.0	602.0
373	G137	9333.0	467.0
374	G139	9315.0	602.0
375	G141	9297.0	467.0
376	G143	9279.0	602.0
377	G145	9261.0	467.0
378	G147	9243.0	602.0
379	G149	9225.0	467.0
380	G151	9207.0	602.0
381	G153	9189.0	467.0
382	G155	9171.0	602.0
383	G157	9153.0	467.0
384	G159	9135.0	602.0
385	G161	9117.0	467.0
386	G163	9099.0	602.0
387	G165	9081.0	467.0
388	G167	9063.0	602.0
389	G169	9045.0	467.0
390	G171	9027.0	602.0
391	G173	9009.0	467.0
392	G175	8991.0	602.0
393	G177	8973.0	467.0
394	G179	8955.0	602.0
395	G181	8937.0	467.0
396	G183	8919.0	602.0
397	G185	8901.0	467.0
398	G187	8883.0	602.0
399	G189	8865.0	467.0
400	G191	8847.0	602.0

R61509 Pad Coordinate（Unit:μm）

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pad No	pad name	X	Y
401	G193	8829.0	467.0
402	G195	8811.0	602.0
403	G197	8793.0	467.0
404	G199	8775.0	602.0
405	G201	8757.0	467.0
406	G203	8739.0	602.0
407	G205	8721.0	467.0
408	G207	8703.0	602.0
409	G209	8685.0	467.0
410	G211	8667.0	602.0
411	G213	8649.0	467.0
412	G215	8631.0	602.0
413	G217	8613.0	467.0
414	G219	8595.0	602.0
415	G221	8577.0	467.0
416	G223	8559.0	602.0
417	G225	8541.0	467.0
418	G227	8523.0	602.0
419	G229	8505.0	467.0
420	G231	8487.0	602.0
421	G233	8469.0	467.0
422	G235	8451.0	602.0
423	G237	8433.0	467.0
424	G239	8415.0	602.0
425	G241	8397.0	467.0
426	G243	8379.0	602.0
427	G245	8361.0	467.0
428	G247	8343.0	602.0
429	G249	8325.0	467.0
430	G251	8307.0	602.0
431	G253	8289.0	467.0
432	G255	8271.0	602.0
433	G257	8253.0	467.0
434	G259	8235.0	602.0
435	G261	8217.0	467.0
436	G263	8199.0	602.0
437	G265	8181.0	467.0
438	G267	8163.0	602.0
439	G269	8145.0	467.0
440	G271	8127.0	602.0
441	G273	8109.0	467.0
442	G275	8091.0	602.0
443	G277	8073.0	467.0
444	G279	8055.0	602.0
445	G281	8037.0	467.0
446	G283	8019.0	602.0
447	G285	8001.0	467.0
448	G287	7983.0	602.0
449	G289	7965.0	467.0
450	G291	7947.0	602.0

pad No	pad name	X	Y
451	G293	7929.0	467.0
452	G295	7911.0	602.0
453	G297	7893.0	467.0
454	G299	7875.0	602.0
455	G301	7857.0	467.0
456	G303	7839.0	602.0
457	G305	7821.0	467.0
458	G307	7803.0	602.0
459	G309	7785.0	467.0
460	G311	7767.0	602.0
461	G313	7749.0	467.0
462	G315	7731.0	602.0
463	G317	7713.0	467.0
464	G319	7695.0	602.0
465	G321	7677.0	467.0
466	G323	7659.0	602.0
467	G325	7641.0	467.0
468	G327	7623.0	602.0
469	G329	7605.0	467.0
470	G331	7587.0	602.0
471	G333	7569.0	467.0
472	G335	7551.0	602.0
473	G337	7533.0	467.0
474	G339	7515.0	602.0
475	G341	7497.0	467.0
476	G343	7479.0	602.0
477	G345	7461.0	467.0
478	G347	7443.0	602.0
479	G349	7425.0	467.0
480	G351	7407.0	602.0
481	G353	7389.0	467.0
482	G355	7371.0	602.0
483	G357	7353.0	467.0
484	G359	7335.0	602.0
485	G361	7317.0	467.0
486	G363	7299.0	602.0
487	G365	7281.0	467.0
488	G367	7263.0	602.0
489	G369	7245.0	467.0
490	G371	7227.0	602.0
491	G373	7209.0	467.0
492	G375	7191.0	602.0
493	G377	7173.0	467.0
494	G379	7155.0	602.0
495	G381	7137.0	467.0
496	G383	7119.0	602.0
497	G385	7101.0	467.0
498	G387	7083.0	602.0
499	G389	7065.0	467.0
500	G391	7047.0	602.0

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pad No	pad name	X	Y
501	G393	7029.0	467.0
502	G395	7011.0	602.0
503	G397	6993.0	467.0
504	G399	6975.0	602.0
505	G401	6957.0	467.0
506	G403	6939.0	602.0
507	G405	6921.0	467.0
508	G407	6903.0	602.0
509	G409	6885.0	467.0
510	G411	6867.0	602.0
511	G413	6849.0	467.0
512	G415	6831.0	602.0
513	G417	6813.0	467.0
514	G419	6795.0	602.0
515	G421	6777.0	467.0
516	G423	6759.0	602.0
517	G425	6741.0	467.0
518	G427	6723.0	602.0
519	G429	6705.0	467.0
520	G431	6687.0	602.0
521	VGLDMY2	6669.0	467.0
522	TESTO13	6651.0	602.0
523	TESTO14	6417.0	602.0
524	S720	6399.0	467.0
525	S719	6381.0	602.0
526	S718	6363.0	467.0
527	S717	6345.0	602.0
528	S716	6327.0	467.0
529	S715	6309.0	602.0
530	S714	6291.0	467.0
531	S713	6273.0	602.0
532	S712	6255.0	467.0
533	S711	6237.0	602.0
534	S710	6219.0	467.0
535	S709	6201.0	602.0
536	S708	6183.0	467.0
537	S707	6165.0	602.0
538	S706	6147.0	467.0
539	S705	6129.0	602.0
540	S704	6111.0	467.0
541	S703	6093.0	602.0
542	S702	6075.0	467.0
543	S701	6057.0	602.0
544	S700	6039.0	467.0
545	S699	6021.0	602.0
546	S698	6003.0	467.0
547	S697	5985.0	602.0
548	S696	5967.0	467.0
549	S695	5949.0	602.0
550	S694	5931.0	467.0

pad No	pad name	X	Y
551	S693	5913.0	602.0
552	S692	5895.0	467.0
553	S691	5877.0	602.0
554	S690	5859.0	467.0
555	S689	5841.0	602.0
556	S688	5823.0	467.0
557	S687	5805.0	602.0
558	S686	5787.0	467.0
559	S685	5769.0	602.0
560	S684	5751.0	467.0
561	S683	5733.0	602.0
562	S682	5715.0	467.0
563	S681	5697.0	602.0
564	S680	5679.0	467.0
565	S679	5661.0	602.0
566	S678	5643.0	467.0
567	S677	5625.0	602.0
568	S676	5607.0	467.0
569	S675	5589.0	602.0
570	S674	5571.0	467.0
571	S673	5553.0	602.0
572	S672	5535.0	467.0
573	S671	5517.0	602.0
574	S670	5499.0	467.0
575	S669	5481.0	602.0
576	S668	5463.0	467.0
577	S667	5445.0	602.0
578	S666	5427.0	467.0
579	S665	5409.0	602.0
580	S664	5391.0	467.0
581	S663	5373.0	602.0
582	S662	5355.0	467.0
583	S661	5337.0	602.0
584	S660	5319.0	467.0
585	S659	5301.0	602.0
586	S658	5283.0	467.0
587	S657	5265.0	602.0
588	S656	5247.0	467.0
589	S655	5229.0	602.0
590	S654	5211.0	467.0
591	S653	5193.0	602.0
592	S652	5175.0	467.0
593	S651	5157.0	602.0
594	S650	5139.0	467.0
595	S649	5121.0	602.0
596	S648	5103.0	467.0
597	S647	5085.0	602.0
598	S646	5067.0	467.0
599	S645	5049.0	602.0
600	S644	5031.0	467.0

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pad No	pad name	X	Y
601	S643	5013.0	602.0
602	S642	4995.0	467.0
603	S641	4977.0	602.0
604	S640	4959.0	467.0
605	S639	4941.0	602.0
606	S638	4923.0	467.0
607	S637	4905.0	602.0
608	S636	4887.0	467.0
609	S635	4869.0	602.0
610	S634	4851.0	467.0
611	S633	4833.0	602.0
612	S632	4815.0	467.0
613	S631	4797.0	602.0
614	S630	4779.0	467.0
615	S629	4761.0	602.0
616	S628	4743.0	467.0
617	S627	4725.0	602.0
618	S626	4707.0	467.0
619	S625	4689.0	602.0
620	S624	4671.0	467.0
621	S623	4653.0	602.0
622	S622	4635.0	467.0
623	S621	4617.0	602.0
624	S620	4599.0	467.0
625	S619	4581.0	602.0
626	S618	4563.0	467.0
627	S617	4545.0	602.0
628	S616	4527.0	467.0
629	S615	4509.0	602.0
630	S614	4491.0	467.0
631	S613	4473.0	602.0
632	S612	4455.0	467.0
633	S611	4437.0	602.0
634	S610	4419.0	467.0
635	S609	4401.0	602.0
636	S608	4383.0	467.0
637	S607	4365.0	602.0
638	S606	4347.0	467.0
639	S605	4329.0	602.0
640	S604	4311.0	467.0
641	S603	4293.0	602.0
642	S602	4275.0	467.0
643	S601	4257.0	602.0
644	S600	4239.0	467.0
645	S599	4221.0	602.0
646	S598	4203.0	467.0
647	S597	4185.0	602.0
648	S596	4167.0	467.0
649	S595	4149.0	602.0
650	S594	4131.0	467.0

pad No	pad name	X	Y
651	S593	4113.0	602.0
652	S592	4095.0	467.0
653	S591	4077.0	602.0
654	S590	4059.0	467.0
655	S589	4041.0	602.0
656	S588	4023.0	467.0
657	S587	4005.0	602.0
658	S586	3987.0	467.0
659	S585	3969.0	602.0
660	S584	3951.0	467.0
661	S583	3933.0	602.0
662	S582	3915.0	467.0
663	S581	3897.0	602.0
664	S580	3879.0	467.0
665	S579	3861.0	602.0
666	S578	3843.0	467.0
667	S577	3825.0	602.0
668	S576	3807.0	467.0
669	S575	3789.0	602.0
670	S574	3771.0	467.0
671	S573	3753.0	602.0
672	S572	3735.0	467.0
673	S571	3717.0	602.0
674	S570	3699.0	467.0
675	S569	3681.0	602.0
676	S568	3663.0	467.0
677	S567	3645.0	602.0
678	S566	3627.0	467.0
679	S565	3609.0	602.0
680	S564	3591.0	467.0
681	S563	3573.0	602.0
682	S562	3555.0	467.0
683	S561	3537.0	602.0
684	S560	3519.0	467.0
685	S559	3501.0	602.0
686	S558	3483.0	467.0
687	S557	3465.0	602.0
688	S556	3447.0	467.0
689	S555	3429.0	602.0
690	S554	3411.0	467.0
691	S553	3393.0	602.0
692	S552	3375.0	467.0
693	S551	3357.0	602.0
694	S550	3339.0	467.0
695	S549	3321.0	602.0
696	S548	3303.0	467.0
697	S547	3285.0	602.0
698	S546	3267.0	467.0
699	S545	3249.0	602.0
700	S544	3231.0	467.0

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pad No	pad name	X	Y
701	S543	3213.0	602.0
702	S542	3195.0	467.0
703	S541	3177.0	602.0
704	S540	3159.0	467.0
705	S539	3141.0	602.0
706	S538	3123.0	467.0
707	S537	3105.0	602.0
708	S536	3087.0	467.0
709	S535	3069.0	602.0
710	S534	3051.0	467.0
711	S533	3033.0	602.0
712	S532	3015.0	467.0
713	S531	2997.0	602.0
714	S530	2979.0	467.0
715	S529	2961.0	602.0
716	S528	2943.0	467.0
717	S527	2925.0	602.0
718	S526	2907.0	467.0
719	S525	2889.0	602.0
720	S524	2871.0	467.0
721	S523	2853.0	602.0
722	S522	2835.0	467.0
723	S521	2817.0	602.0
724	S520	2799.0	467.0
725	S519	2781.0	602.0
726	S518	2763.0	467.0
727	S517	2745.0	602.0
728	S516	2727.0	467.0
729	S515	2709.0	602.0
730	S514	2691.0	467.0
731	S513	2673.0	602.0
732	S512	2655.0	467.0
733	S511	2637.0	602.0
734	S510	2619.0	467.0
735	S509	2601.0	602.0
736	S508	2583.0	467.0
737	S507	2565.0	602.0
738	S506	2547.0	467.0
739	S505	2529.0	602.0
740	S504	2511.0	467.0
741	S503	2493.0	602.0
742	S502	2475.0	467.0
743	S501	2457.0	602.0
744	S500	2439.0	467.0
745	S499	2421.0	602.0
746	S498	2403.0	467.0
747	S497	2385.0	602.0
748	S496	2367.0	467.0
749	S495	2349.0	602.0
750	S494	2331.0	467.0

pad No	pad name	X	Y
751	S493	2313.0	602.0
752	S492	2295.0	467.0
753	S491	2277.0	602.0
754	S490	2259.0	467.0
755	S489	2241.0	602.0
756	S488	2223.0	467.0
757	S487	2205.0	602.0
758	S486	2187.0	467.0
759	S485	2169.0	602.0
760	S484	2151.0	467.0
761	S483	2133.0	602.0
762	S482	2115.0	467.0
763	S481	2097.0	602.0
764	S480	2079.0	467.0
765	S479	2061.0	602.0
766	S478	2043.0	467.0
767	S477	2025.0	602.0
768	S476	2007.0	467.0
769	S475	1989.0	602.0
770	S474	1971.0	467.0
771	S473	1953.0	602.0
772	S472	1935.0	467.0
773	S471	1917.0	602.0
774	S470	1899.0	467.0
775	S469	1881.0	602.0
776	S468	1863.0	467.0
777	S467	1845.0	602.0
778	S466	1827.0	467.0
779	S465	1809.0	602.0
780	S464	1791.0	467.0
781	S463	1773.0	602.0
782	S462	1755.0	467.0
783	S461	1737.0	602.0
784	S460	1719.0	467.0
785	S459	1701.0	602.0
786	S458	1683.0	467.0
787	S457	1665.0	602.0
788	S456	1647.0	467.0
789	S455	1629.0	602.0
790	S454	1611.0	467.0
791	S453	1593.0	602.0
792	S452	1575.0	467.0
793	S451	1557.0	602.0
794	S450	1539.0	467.0
795	S449	1521.0	602.0
796	S448	1503.0	467.0
797	S447	1485.0	602.0
798	S446	1467.0	467.0
799	S445	1449.0	602.0
800	S444	1431.0	467.0

R61509 Pad Coordinate（Unit:μm）

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pad No	pad name	X	Y
801	S443	1413.0	602.0
802	S442	1395.0	467.0
803	S441	1377.0	602.0
804	S440	1359.0	467.0
805	S439	1341.0	602.0
806	S438	1323.0	467.0
807	S437	1305.0	602.0
808	S436	1287.0	467.0
809	S435	1269.0	602.0
810	S434	1251.0	467.0
811	S433	1233.0	602.0
812	S432	1215.0	467.0
813	S431	1197.0	602.0
814	S430	1179.0	467.0
815	S429	1161.0	602.0
816	S428	1143.0	467.0
817	S427	1125.0	602.0
818	S426	1107.0	467.0
819	S425	1089.0	602.0
820	S424	1071.0	467.0
821	S423	1053.0	602.0
822	S422	1035.0	467.0
823	S421	1017.0	602.0
824	S420	999.0	467.0
825	S419	981.0	602.0
826	S418	963.0	467.0
827	S417	945.0	602.0
828	S416	927.0	467.0
829	S415	909.0	602.0
830	S414	891.0	467.0
831	S413	873.0	602.0
832	S412	855.0	467.0
833	S411	837.0	602.0
834	S410	819.0	467.0
835	S409	801.0	602.0
836	S408	783.0	467.0
837	S407	765.0	602.0
838	S406	747.0	467.0
839	S405	729.0	602.0
840	S404	711.0	467.0
841	S403	693.0	602.0
842	S402	675.0	467.0
843	S401	657.0	602.0
844	S400	639.0	467.0
845	S399	621.0	602.0
846	S398	603.0	467.0
847	S397	585.0	602.0
848	S396	567.0	467.0
849	S395	549.0	602.0
850	S394	531.0	467.0

pad No	pad name	X	Y
851	S393	513.0	602.0
852	S392	495.0	467.0
853	S391	477.0	602.0
854	S390	459.0	467.0
855	S389	441.0	602.0
856	S388	423.0	467.0
857	S387	405.0	602.0
858	S386	387.0	467.0
859	S385	369.0	602.0
860	S384	351.0	467.0
861	S383	333.0	602.0
862	S382	315.0	467.0
863	S381	297.0	602.0
864	S380	279.0	467.0
865	S379	261.0	602.0
866	S378	243.0	467.0
867	S377	225.0	602.0
868	S376	207.0	467.0
869	S375	189.0	602.0
870	S374	171.0	467.0
871	S373	153.0	602.0
872	S372	135.0	467.0
873	S371	117.0	602.0
874	S370	99.0	467.0
875	S369	81.0	602.0
876	S368	63.0	467.0
877	S367	45.0	602.0
878	S366	27.0	467.0
879	S365	9.0	602.0
880	S364	-9.0	467.0
881	S363	-27.0	602.0
882	S362	-45.0	467.0
883	S361	-63.0	602.0
884	S360	-81.0	467.0
885	S359	-99.0	602.0
886	S358	-117.0	467.0
887	S357	-135.0	602.0
888	S356	-153.0	467.0
889	S355	-171.0	602.0
890	S354	-189.0	467.0
891	S353	-207.0	602.0
892	S352	-225.0	467.0
893	S351	-243.0	602.0
894	S350	-261.0	467.0
895	S349	-279.0	602.0
896	S348	-297.0	467.0
897	S347	-315.0	602.0
898	S346	-333.0	467.0
899	S345	-351.0	602.0
900	S344	-369.0	467.0

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pad No	pad name	X	Y
901	S343	-387.0	602.0
902	S342	-405.0	467.0
903	S341	-423.0	602.0
904	S340	-441.0	467.0
905	S339	-459.0	602.0
906	S338	-477.0	467.0
907	S337	-495.0	602.0
908	S336	-513.0	467.0
909	S335	-531.0	602.0
910	S334	-549.0	467.0
911	S333	-567.0	602.0
912	S332	-585.0	467.0
913	S331	-603.0	602.0
914	S330	-621.0	467.0
915	S329	-639.0	602.0
916	S328	-657.0	467.0
917	S327	-675.0	602.0
918	S326	-693.0	467.0
919	S325	-711.0	602.0
920	S324	-729.0	467.0
921	S323	-747.0	602.0
922	S322	-765.0	467.0
923	S321	-783.0	602.0
924	S320	-801.0	467.0
925	S319	-819.0	602.0
926	S318	-837.0	467.0
927	S317	-855.0	602.0
928	S316	-873.0	467.0
929	S315	-891.0	602.0
930	S314	-909.0	467.0
931	S313	-927.0	602.0
932	S312	-945.0	467.0
933	S311	-963.0	602.0
934	S310	-981.0	467.0
935	S309	-999.0	602.0
936	S308	-1017.0	467.0
937	S307	-1035.0	602.0
938	S306	-1053.0	467.0
939	S305	-1071.0	602.0
940	S304	-1089.0	467.0
941	S303	-1107.0	602.0
942	S302	-1125.0	467.0
943	S301	-1143.0	602.0
944	S300	-1161.0	467.0
945	S299	-1179.0	602.0
946	S298	-1197.0	467.0
947	S297	-1215.0	602.0
948	S296	-1233.0	467.0
949	S295	-1251.0	602.0
950	S294	-1269.0	467.0

pad No	pad name	X	Y
951	S293	-1287.0	602.0
952	S292	-1305.0	467.0
953	S291	-1323.0	602.0
954	S290	-1341.0	467.0
955	S289	-1359.0	602.0
956	S288	-1377.0	467.0
957	S287	-1395.0	602.0
958	S286	-1413.0	467.0
959	S285	-1431.0	602.0
960	S284	-1449.0	467.0
961	S283	-1467.0	602.0
962	S282	-1485.0	467.0
963	S281	-1503.0	602.0
964	S280	-1521.0	467.0
965	S279	-1539.0	602.0
966	S278	-1557.0	467.0
967	S277	-1575.0	602.0
968	S276	-1593.0	467.0
969	S275	-1611.0	602.0
970	S274	-1629.0	467.0
971	S273	-1647.0	602.0
972	S272	-1665.0	467.0
973	S271	-1683.0	602.0
974	S270	-1701.0	467.0
975	S269	-1719.0	602.0
976	S268	-1737.0	467.0
977	S267	-1755.0	602.0
978	S266	-1773.0	467.0
979	S265	-1791.0	602.0
980	S264	-1809.0	467.0
981	S263	-1827.0	602.0
982	S262	-1845.0	467.0
983	S261	-1863.0	602.0
984	S260	-1881.0	467.0
985	S259	-1899.0	602.0
986	S258	-1917.0	467.0
987	S257	-1935.0	602.0
988	S256	-1953.0	467.0
989	S255	-1971.0	602.0
990	S254	-1989.0	467.0
991	S253	-2007.0	602.0
992	S252	-2025.0	467.0
993	S251	-2043.0	602.0
994	S250	-2061.0	467.0
995	S249	-2079.0	602.0
996	S248	-2097.0	467.0
997	S247	-2115.0	602.0
998	S246	-2133.0	467.0
999	S245	-2151.0	602.0
1000	S244	-2169.0	467.0

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pad No	pad name	X	Y
1001	S243	-2187.0	602.0
1002	S242	-2205.0	467.0
1003	S241	-2223.0	602.0
1004	S240	-2241.0	467.0
1005	S239	-2259.0	602.0
1006	S238	-2277.0	467.0
1007	S237	-2295.0	602.0
1008	S236	-2313.0	467.0
1009	S235	-2331.0	602.0
1010	S234	-2349.0	467.0
1011	S233	-2367.0	602.0
1012	S232	-2385.0	467.0
1013	S231	-2403.0	602.0
1014	S230	-2421.0	467.0
1015	S229	-2439.0	602.0
1016	S228	-2457.0	467.0
1017	S227	-2475.0	602.0
1018	S226	-2493.0	467.0
1019	S225	-2511.0	602.0
1020	S224	-2529.0	467.0
1021	S223	-2547.0	602.0
1022	S222	-2565.0	467.0
1023	S221	-2583.0	602.0
1024	S220	-2601.0	467.0
1025	S219	-2619.0	602.0
1026	S218	-2637.0	467.0
1027	S217	-2655.0	602.0
1028	S216	-2673.0	467.0
1029	S215	-2691.0	602.0
1030	S214	-2709.0	467.0
1031	S213	-2727.0	602.0
1032	S212	-2745.0	467.0
1033	S211	-2763.0	602.0
1034	S210	-2781.0	467.0
1035	S209	-2799.0	602.0
1036	S208	-2817.0	467.0
1037	S207	-2835.0	602.0
1038	S206	-2853.0	467.0
1039	S205	-2871.0	602.0
1040	S204	-2889.0	467.0
1041	S203	-2907.0	602.0
1042	S202	-2925.0	467.0
1043	S201	-2943.0	602.0
1044	S200	-2961.0	467.0
1045	S199	-2979.0	602.0
1046	S198	-2997.0	467.0
1047	S197	-3015.0	602.0
1048	S196	-3033.0	467.0
1049	S195	-3051.0	602.0
1050	S194	-3069.0	467.0

pad No	pad name	X	Y
1051	S193	-3087.0	602.0
1052	S192	-3105.0	467.0
1053	S191	-3123.0	602.0
1054	S190	-3141.0	467.0
1055	S189	-3159.0	602.0
1056	S188	-3177.0	467.0
1057	S187	-3195.0	602.0
1058	S186	-3213.0	467.0
1059	S185	-3231.0	602.0
1060	S184	-3249.0	467.0
1061	S183	-3267.0	602.0
1062	S182	-3285.0	467.0
1063	S181	-3303.0	602.0
1064	S180	-3321.0	467.0
1065	S179	-3339.0	602.0
1066	S178	-3357.0	467.0
1067	S177	-3375.0	602.0
1068	S176	-3393.0	467.0
1069	S175	-3411.0	602.0
1070	S174	-3429.0	467.0
1071	S173	-3447.0	602.0
1072	S172	-3465.0	467.0
1073	S171	-3483.0	602.0
1074	S170	-3501.0	467.0
1075	S169	-3519.0	602.0
1076	S168	-3537.0	467.0
1077	S167	-3555.0	602.0
1078	S166	-3573.0	467.0
1079	S165	-3591.0	602.0
1080	S164	-3609.0	467.0
1081	S163	-3627.0	602.0
1082	S162	-3645.0	467.0
1083	S161	-3663.0	602.0
1084	S160	-3681.0	467.0
1085	S159	-3699.0	602.0
1086	S158	-3717.0	467.0
1087	S157	-3735.0	602.0
1088	S156	-3753.0	467.0
1089	S155	-3771.0	602.0
1090	S154	-3789.0	467.0
1091	S153	-3807.0	602.0
1092	S152	-3825.0	467.0
1093	S151	-3843.0	602.0
1094	S150	-3861.0	467.0
1095	S149	-3879.0	602.0
1096	S148	-3897.0	467.0
1097	S147	-3915.0	602.0
1098	S146	-3933.0	467.0
1099	S145	-3951.0	602.0
1100	S144	-3969.0	467.0

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pad No	pad name	X	Y
1101	S143	-3987.0	602.0
1102	S142	-4005.0	467.0
1103	S141	-4023.0	602.0
1104	S140	-4041.0	467.0
1105	S139	-4059.0	602.0
1106	S138	-4077.0	467.0
1107	S137	-4095.0	602.0
1108	S136	-4113.0	467.0
1109	S135	-4131.0	602.0
1110	S134	-4149.0	467.0
1111	S133	-4167.0	602.0
1112	S132	-4185.0	467.0
1113	S131	-4203.0	602.0
1114	S130	-4221.0	467.0
1115	S129	-4239.0	602.0
1116	S128	-4257.0	467.0
1117	S127	-4275.0	602.0
1118	S126	-4293.0	467.0
1119	S125	-4311.0	602.0
1120	S124	-4329.0	467.0
1121	S123	-4347.0	602.0
1122	S122	-4365.0	467.0
1123	S121	-4383.0	602.0
1124	S120	-4401.0	467.0
1125	S119	-4419.0	602.0
1126	S118	-4437.0	467.0
1127	S117	-4455.0	602.0
1128	S116	-4473.0	467.0
1129	S115	-4491.0	602.0
1130	S114	-4509.0	467.0
1131	S113	-4527.0	602.0
1132	S112	-4545.0	467.0
1133	S111	-4563.0	602.0
1134	S110	-4581.0	467.0
1135	S109	-4599.0	602.0
1136	S108	-4617.0	467.0
1137	S107	-4635.0	602.0
1138	S106	-4653.0	467.0
1139	S105	-4671.0	602.0
1140	S104	-4689.0	467.0
1141	S103	-4707.0	602.0
1142	S102	-4725.0	467.0
1143	S101	-4743.0	602.0
1144	S100	-4761.0	467.0
1145	S99	-4779.0	602.0
1146	S98	-4797.0	467.0
1147	S97	-4815.0	602.0
1148	S96	-4833.0	467.0
1149	S95	-4851.0	602.0
1150	S94	-4869.0	467.0

pad No	pad name	X	Y
1151	S93	-4887.0	602.0
1152	S92	-4905.0	467.0
1153	S91	-4923.0	602.0
1154	S90	-4941.0	467.0
1155	S89	-4959.0	602.0
1156	S88	-4977.0	467.0
1157	S87	-4995.0	602.0
1158	S86	-5013.0	467.0
1159	S85	-5031.0	602.0
1160	S84	-5049.0	467.0
1161	S83	-5067.0	602.0
1162	S82	-5085.0	467.0
1163	S81	-5103.0	602.0
1164	S80	-5121.0	467.0
1165	S79	-5139.0	602.0
1166	S78	-5157.0	467.0
1167	S77	-5175.0	602.0
1168	S76	-5193.0	467.0
1169	S75	-5211.0	602.0
1170	S74	-5229.0	467.0
1171	S73	-5247.0	602.0
1172	S72	-5265.0	467.0
1173	S71	-5283.0	602.0
1174	S70	-5301.0	467.0
1175	S69	-5319.0	602.0
1176	S68	-5337.0	467.0
1177	S67	-5355.0	602.0
1178	S66	-5373.0	467.0
1179	S65	-5391.0	602.0
1180	S64	-5409.0	467.0
1181	S63	-5427.0	602.0
1182	S62	-5445.0	467.0
1183	S61	-5463.0	602.0
1184	S60	-5481.0	467.0
1185	S59	-5499.0	602.0
1186	S58	-5517.0	467.0
1187	S57	-5535.0	602.0
1188	S56	-5553.0	467.0
1189	S55	-5571.0	602.0
1190	S54	-5589.0	467.0
1191	S53	-5607.0	602.0
1192	S52	-5625.0	467.0
1193	S51	-5643.0	602.0
1194	S50	-5661.0	467.0
1195	S49	-5679.0	602.0
1196	S48	-5697.0	467.0
1197	S47	-5715.0	602.0
1198	S46	-5733.0	467.0
1199	S45	-5751.0	602.0
1200	S44	-5769.0	467.0

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pad No	pad name	X	Y
1201	S43	-5787.0	602.0
1202	S42	-5805.0	467.0
1203	S41	-5823.0	602.0
1204	S40	-5841.0	467.0
1205	S39	-5859.0	602.0
1206	S38	-5877.0	467.0
1207	S37	-5895.0	602.0
1208	S36	-5913.0	467.0
1209	S35	-5931.0	602.0
1210	S34	-5949.0	467.0
1211	S33	-5967.0	602.0
1212	S32	-5985.0	467.0
1213	S31	-6003.0	602.0
1214	S30	-6021.0	467.0
1215	S29	-6039.0	602.0
1216	S28	-6057.0	467.0
1217	S27	-6075.0	602.0
1218	S26	-6093.0	467.0
1219	S25	-6111.0	602.0
1220	S24	-6129.0	467.0
1221	S23	-6147.0	602.0
1222	S22	-6165.0	467.0
1223	S21	-6183.0	602.0
1224	S20	-6201.0	467.0
1225	S19	-6219.0	602.0
1226	S18	-6237.0	467.0
1227	S17	-6255.0	602.0
1228	S16	-6273.0	467.0
1229	S15	-6291.0	602.0
1230	S14	-6309.0	467.0
1231	S13	-6327.0	602.0
1232	S12	-6345.0	467.0
1233	S11	-6363.0	602.0
1234	S10	-6381.0	467.0
1235	S9	-6399.0	602.0
1236	S8	-6417.0	467.0
1237	S7	-6435.0	602.0
1238	S6	-6453.0	467.0
1239	S5	-6471.0	602.0
1240	S4	-6489.0	467.0
1241	S3	-6507.0	602.0
1242	S2	-6525.0	467.0
1243	S1	-6543.0	602.0
1244	TESTO15	-6561.0	467.0
1245	TESTO16	-6651.0	602.0
1246	VGLDMY3	-6669.0	467.0
1247	G432	-6687.0	602.0
1248	G430	-6705.0	467.0
1249	G428	-6723.0	602.0
1250	G426	-6741.0	467.0

pad No	pad name	X	Y
1251	G424	-6759.0	602.0
1252	G422	-6777.0	467.0
1253	G420	-6795.0	602.0
1254	G418	-6813.0	467.0
1255	G416	-6831.0	602.0
1256	G414	-6849.0	467.0
1257	G412	-6867.0	602.0
1258	G410	-6885.0	467.0
1259	G408	-6903.0	602.0
1260	G406	-6921.0	467.0
1261	G404	-6939.0	602.0
1262	G402	-6957.0	467.0
1263	G400	-6975.0	602.0
1264	G398	-6993.0	467.0
1265	G396	-7011.0	602.0
1266	G394	-7029.0	467.0
1267	G392	-7047.0	602.0
1268	G390	-7065.0	467.0
1269	G388	-7083.0	602.0
1270	G386	-7101.0	467.0
1271	G384	-7119.0	602.0
1272	G382	-7137.0	467.0
1273	G380	-7155.0	602.0
1274	G378	-7173.0	467.0
1275	G376	-7191.0	602.0
1276	G374	-7209.0	467.0
1277	G372	-7227.0	602.0
1278	G370	-7245.0	467.0
1279	G368	-7263.0	602.0
1280	G366	-7281.0	467.0
1281	G364	-7299.0	602.0
1282	G362	-7317.0	467.0
1283	G360	-7335.0	602.0
1284	G358	-7353.0	467.0
1285	G356	-7371.0	602.0
1286	G354	-7389.0	467.0
1287	G352	-7407.0	602.0
1288	G350	-7425.0	467.0
1289	G348	-7443.0	602.0
1290	G346	-7461.0	467.0
1291	G344	-7479.0	602.0
1292	G342	-7497.0	467.0
1293	G340	-7515.0	602.0
1294	G338	-7533.0	467.0
1295	G336	-7551.0	602.0
1296	G334	-7569.0	467.0
1297	G332	-7587.0	602.0
1298	G330	-7605.0	467.0
1299	G328	-7623.0	602.0
1300	G326	-7641.0	467.0

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pad No	pad name	X	Y
1301	G324	-7659.0	602.0
1302	G322	-7677.0	467.0
1303	G320	-7695.0	602.0
1304	G318	-7713.0	467.0
1305	G316	-7731.0	602.0
1306	G314	-7749.0	467.0
1307	G312	-7767.0	602.0
1308	G310	-7785.0	467.0
1309	G308	-7803.0	602.0
1310	G306	-7821.0	467.0
1311	G304	-7839.0	602.0
1312	G302	-7857.0	467.0
1313	G300	-7875.0	602.0
1314	G298	-7893.0	467.0
1315	G296	-7911.0	602.0
1316	G294	-7929.0	467.0
1317	G292	-7947.0	602.0
1318	G290	-7965.0	467.0
1319	G288	-7983.0	602.0
1320	G286	-8001.0	467.0
1321	G284	-8019.0	602.0
1322	G282	-8037.0	467.0
1323	G280	-8055.0	602.0
1324	G278	-8073.0	467.0
1325	G276	-8091.0	602.0
1326	G274	-8109.0	467.0
1327	G272	-8127.0	602.0
1328	G270	-8145.0	467.0
1329	G268	-8163.0	602.0
1330	G266	-8181.0	467.0
1331	G264	-8199.0	602.0
1332	G262	-8217.0	467.0
1333	G260	-8235.0	602.0
1334	G258	-8253.0	467.0
1335	G256	-8271.0	602.0
1336	G254	-8289.0	467.0
1337	G252	-8307.0	602.0
1338	G250	-8325.0	467.0
1339	G248	-8343.0	602.0
1340	G246	-8361.0	467.0
1341	G244	-8379.0	602.0
1342	G242	-8397.0	467.0
1343	G240	-8415.0	602.0
1344	G238	-8433.0	467.0
1345	G236	-8451.0	602.0
1346	G234	-8469.0	467.0
1347	G232	-8487.0	602.0
1348	G230	-8505.0	467.0
1349	G228	-8523.0	602.0
1350	G226	-8541.0	467.0

pad No	pad name	X	Y
1351	G224	-8559.0	602.0
1352	G222	-8577.0	467.0
1353	G220	-8595.0	602.0
1354	G218	-8613.0	467.0
1355	G216	-8631.0	602.0
1356	G214	-8649.0	467.0
1357	G212	-8667.0	602.0
1358	G210	-8685.0	467.0
1359	G208	-8703.0	602.0
1360	G206	-8721.0	467.0
1361	G204	-8739.0	602.0
1362	G202	-8757.0	467.0
1363	G200	-8775.0	602.0
1364	G198	-8793.0	467.0
1365	G196	-8811.0	602.0
1366	G194	-8829.0	467.0
1367	G192	-8847.0	602.0
1368	G190	-8865.0	467.0
1369	G188	-8883.0	602.0
1370	G186	-8901.0	467.0
1371	G184	-8919.0	602.0
1372	G182	-8937.0	467.0
1373	G180	-8955.0	602.0
1374	G178	-8973.0	467.0
1375	G176	-8991.0	602.0
1376	G174	-9009.0	467.0
1377	G172	-9027.0	602.0
1378	G170	-9045.0	467.0
1379	G168	-9063.0	602.0
1380	G166	-9081.0	467.0
1381	G164	-9099.0	602.0
1382	G162	-9117.0	467.0
1383	G160	-9135.0	602.0
1384	G158	-9153.0	467.0
1385	G156	-9171.0	602.0
1386	G154	-9189.0	467.0
1387	G152	-9207.0	602.0
1388	G150	-9225.0	467.0
1389	G148	-9243.0	602.0
1390	G146	-9261.0	467.0
1391	G144	-9279.0	602.0
1392	G142	-9297.0	467.0
1393	G140	-9315.0	602.0
1394	G138	-9333.0	467.0
1395	G136	-9351.0	602.0
1396	G134	-9369.0	467.0
1397	G132	-9387.0	602.0
1398	G130	-9405.0	467.0
1399	G128	-9423.0	602.0
1400	G126	-9441.0	467.0

R61509 Pad Coordinate（Unit:μm）

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pad No	pad name	X	Y
1401	G124	-9459.0	602.0
1402	G122	-9477.0	467.0
1403	G120	-9495.0	602.0
1404	G118	-9513.0	467.0
1405	G116	-9531.0	602.0
1406	G114	-9549.0	467.0
1407	G112	-9567.0	602.0
1408	G110	-9585.0	467.0
1409	G108	-9603.0	602.0
1410	G106	-9621.0	467.0
1411	G104	-9639.0	602.0
1412	G102	-9657.0	467.0
1413	G100	-9675.0	602.0
1414	G98	-9693.0	467.0
1415	G96	-9711.0	602.0
1416	G94	-9729.0	467.0
1417	G92	-9747.0	602.0
1418	G90	-9765.0	467.0
1419	G88	-9783.0	602.0
1420	G86	-9801.0	467.0
1421	G84	-9819.0	602.0
1422	G82	-9837.0	467.0
1423	G80	-9855.0	602.0
1424	G78	-9873.0	467.0
1425	G76	-9891.0	602.0
1426	G74	-9909.0	467.0
1427	G72	-9927.0	602.0
1428	G70	-9945.0	467.0
1429	G68	-9963.0	602.0
1430	G66	-9981.0	467.0
1431	G64	-9999.0	602.0
1432	G62	-10017.0	467.0
1433	G60	-10035.0	602.0
1434	G58	-10053.0	467.0
1435	G56	-10071.0	602.0
1436	G54	-10089.0	467.0
1437	G52	-10107.0	602.0
1438	G50	-10125.0	467.0
1439	G48	-10143.0	602.0
1440	G46	-10161.0	467.0
1441	G44	-10179.0	602.0
1442	G42	-10197.0	467.0
1443	G40	-10215.0	602.0
1444	G38	-10233.0	467.0
1445	G36	-10251.0	602.0
1446	G34	-10269.0	467.0
1447	G32	-10287.0	602.0
1448	G30	-10305.0	467.0
1449	G28	-10323.0	602.0
1450	G26	-10341.0	467.0

pad No	pad name	X	Y
1451	G24	-10359.0	602.0
1452	G22	-10377.0	467.0
1453	G20	-10395.0	602.0
1454	G18	-10413.0	467.0
1455	G16	-10431.0	602.0
1456	G14	-10449.0	467.0
1457	G12	-10467.0	602.0
1458	G10	-10485.0	467.0
1459	G8	-10503.0	602.0
1460	G6	-10521.0	467.0
1461	G4	-10539.0	602.0
1462	G2	-10557.0	467.0
1463	VGLDMY4	-10575.0	602.0
1464	DUMMYR9	-10593.0	467.0
1465	DUMMYR10	-10611.0	602.0
1466	TESTO17	-10629.0	467.0
1467	TESTO18	-10647.0	602.0

Alignment mark	X	Y
1-a	-10608.0	-548.0
1-b	10608.0	-548.0

Bump arrangement

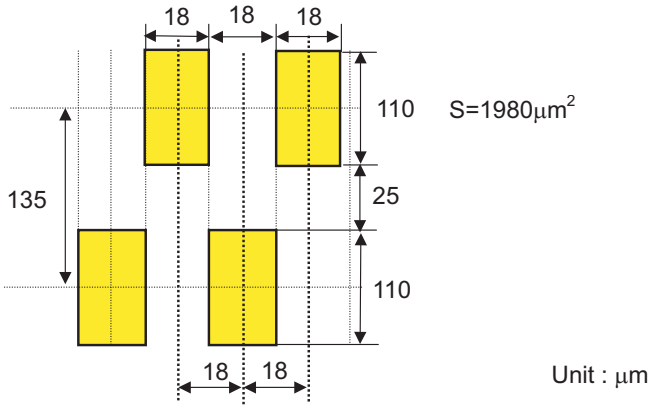
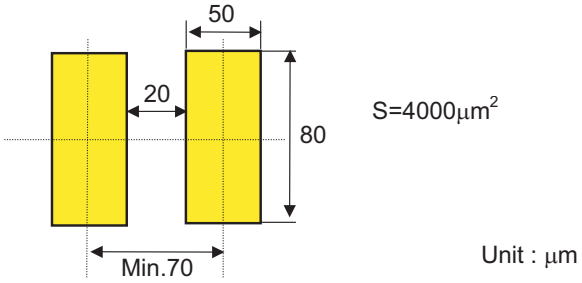
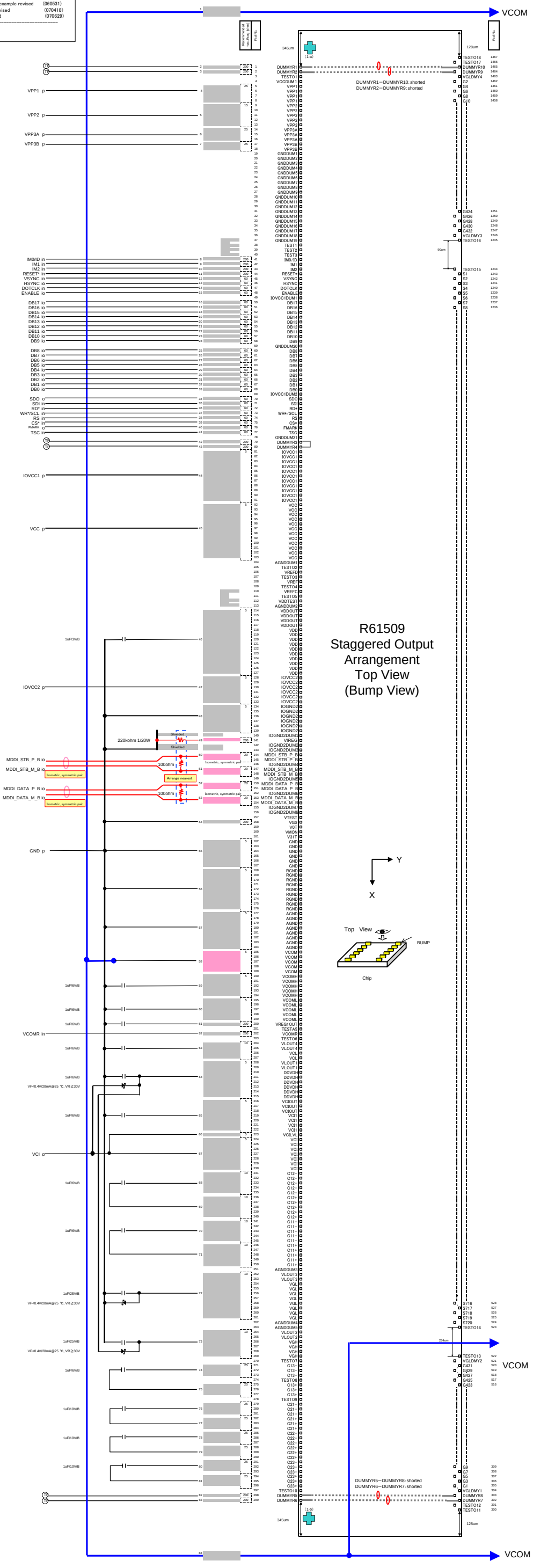
S1-S720, G1-G432, DUMMYR7-10, TESTO11-18, VGLDMY1-4 (No. 300-1467)	
I/O pins **(No1 – 299)**	

Figure 3

R61509 Connection Example

Rev.1.0.4 2007.06.29

Rev0.0	R61509 new release	
Rev0.0.1	R61509 Floor Plan revised	(060428)
Rev1.0	R61509 Specifications decision	(060516)
Rev1.0.1	R61509 Bump Layout revised	(060518)
Rev1.0.2	R61509 connection example revised	(060531)
Rev1.0.3	diode connection revised	(070418)
Rev1.0.4	diode symbol revised	(070629)



GRAM Address Map

Table 12 GRAM address and display position on the panel (SS = 0, BGR = 0)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	· · · · ·	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			· · · · ·	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G432	h00000			h00001			h00002			h00003			· · · · ·	h000EC			h000ED			h000EE			h000EF		
G2	G431	h00100			h00101			h00102			h00103			· · · · ·	h001EC			h001ED			h001EE			h001EF		
G3	G430	h00200			h00201			h00202			h00203			· · · · ·	h002EC			h002ED			h002EE			h002EF		
G4	G429	h00300			h00301			h00302			h00303			· · · · ·	h003EC			h003ED			h003EE			h003EF		
G5	G428	h00400			h00401			h00402			h00403			· · · · ·	h004EC			h004ED			h004EE			h004EF		
G6	G427	h00500			h00501			h00502			h00503			· · · · ·	h005EC			h005ED			h005EE			h005EF		
G7	G426	h00600			h00601			h00602			h00603			· · · · ·	h006EC			h006ED			h006EE			h006EF		
G8	G425	h00700			h00701			h00702			h00703			· · · · ·	h007EC			h007ED			h007EE			h007EF		
G9	G424	h00800			h00801			h00802			h00803			· · · · ·	h008EC			h008ED			h008EE			h008EF		
G10	G423	h00900			h00901			h00902			h00903			· · · · ·	h009EC			h009ED			h009EE			h009EF		
G11	G422	h00A00			h00A01			h00A02			h00A03			· · · · ·	h00AEC			h00AED			h00AEE			h00AEF		
G12	G421	h00B00			h00B01			h00B02			h00B03			· · · · ·	h00BEC			h00BED			h00BEE			h00BEF		
G13	G420	h00C00			h00C01			h00C02			h00C03			· · · · ·	h00CEC			h00CED			h00CEE			h00CEF		
G14	G419	h00D00			h00D01			h00D02			h00D03			· · · · ·	h00DEC			h00DED			h00DEE			h00DEF		
G15	G418	h00E00			h00E01			h00E02			h00E03			· · · · ·	h00EEC			h00EED			h00EEE			h00EEF		
G16	G417	h00F00			h00F01			h00F02			h00F03			· · · · ·	h00FEC			h00FED			h00FEE			h00FEF		
G17	G416	h01000			h01001			h01002			h01003			· · · · ·	h010EC			h010ED			h010EE			h010EF		
G18	G415	h01100			h01101			h01102			h01103			· · · · ·	h011EC			h011ED			h011EE			h011EF		
G19	G414	h01200			h01201			h01202			h01203			· · · · ·	h012EC			h012ED			h012EE			h012EF		
G20	G413	h01300			h01301			h01302			h01303			· · · · ·	h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G417	G16	h1A000			h1A001			h1A002			h1A003			· · · · ·	h1A0EC			h1A0ED			h1A0EE			h1A0EF		
G418	G15	h1A100			h1A101			h1A102			h1A103			· · · · ·	h1A1EC			h1A1ED			h1A1EE			h1A1EF		
G419	G14	h1A200			h1A201			h1A202			h1A203			· · · · ·	h1A2EC			h1A2ED			h1A2EE			h1A2EF		
G420	G13	h1A300			h1A301			h1A302			h1A303			· · · · ·	h1A3EC			h1A3ED			h1A3EE			h1A3EF		
G421	G12	h1A400			h1A401			h1A402			h1A403			· · · · ·	h1A4EC			h1A4ED			h1A4EE			h1A4EF		
G422	G11	h1A500			h1A501			h1A502			h1A503			· · · · ·	h1A5EC			h1A5ED			h1A5EE			h1A5EF		
G423	G10	h1A600			h1A601			h1A602			h1A603			· · · · ·	h1A6EC			h1A6ED			h1A6EE			h1A6EF		
G424	G9	h1A700			h1A701			h1A702			h1A703			· · · · ·	h1A7EC			h1A7ED			h1A7EE			h1A7EF		
G425	G8	h1A800			h1A801			h1A802			h1A803			· · · · ·	h1A8EC			h1A8ED			h1A8EE			h1A8EF		
G426	G7	h1A900			h1A901			h1A902			h1A903			· · · · ·	h1A9EC			h1A9ED			h1A9EE			h1A9EF		
G427	G6	h1AA00			h1AA01			h1AA02			h1AA03			· · · · ·	h1AAEC			h1AAED			h1AAEE			h1AAEF		
G428	G5	h1AB00			h1AB01			h1AB02			h1AB03			· · · · ·	h1ABEC			h1ABED			h1ABEE			h1ABEF		
G429	G4	h1AC00			h1AC01			h1AC02			h1AC03			· · · · ·	h1ACEC			h1ACED			h1ACEE			h1ACEF		
G430	G3	h1AD00			h1AD01			h1AD02			h1AD03			· · · · ·	h1ADEC			h1ADED			h1ADEE			h1ADEF		
G431	G2	h1AE00			h1AE01			h1AE02			h1AE03			· · · · ·	h1AEEC			h1AEED			h1AEEE			h1AEEF		
G432	G1	h1AF00			h1AF01			h1AF02			h1AF03			· · · · ·	h1AFEC			h1AFED			h1AFEE			h1AFEF		

Table 13 GRAM address and display position on the panel (SS = 1, BGR = 1)

S/G pin		S720	S719	S718	S717	S716	S715	S714	S713	S712	S711	S710	S709	· · · · ·	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			· · · · ·	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G432	h00000			h00001			h00002			h00003			· · · · ·	h000EC			h000ED			h000EE			h000EF		
G2	G431	h00100			h00101			h00102			h00103			· · · · ·	h001EC			h001ED			h001EE			h001EF		
G3	G430	h00200			h00201			h00202			h00203			· · · · ·	h002EC			h002ED			h002EE			h002EF		
G4	G429	h00300			h00301			h00302			h00303			· · · · ·	h003EC			h003ED			h003EE			h003EF		
G5	G428	h00400			h00401			h00402			h00403			· · · · ·	h004EC			h004ED			h004EE			h004EF		
G6	G427	h00500			h00501			h00502			h00503			· · · · ·	h005EC			h005ED			h005EE			h005EF		
G7	G426	h00600			h00601			h00602			h00603			· · · · ·	h006EC			h006ED			h006EE			h006EF		
G8	G425	h00700			h00701			h00702			h00703			· · · · ·	h007EC			h007ED			h007EE			h007EF		
G9	G424	h00800			h00801			h00802			h00803			· · · · ·	h008EC			h008ED			h008EE			h008EF		
G10	G423	h00900			h00901			h00902			h00903			· · · · ·	h009EC			h009ED			h009EE			h009EF		
G11	G422	h00A00			h00A01			h00A02			h00A03			· · · · ·	h00AEC			h00AED			h00AEE			h00AEF		
G12	G421	h00B00			h00B01			h00B02			h00B03			· · · · ·	h00BEC			h00BED			h00BEE			h00BEF		
G13	G420	h00C00			h00C01			h00C02			h00C03			· · · · ·	h00CEC			h00CED			h00CEE			h00CEF		
G14	G419	h00D00			h00D01			h00D02			h00D03			· · · · ·	h00DEC			h00DED			h00DEE			h00DEF		
G15	G418	h00E00			h00E01			h00E02			h00E03			· · · · ·	h00EEC			h00EED			h00EEE			h00EEF		
G16	G417	h00F00			h00F01			h00F02			h00F03			· · · · ·	h00FEC			h00FED			h00FEE			h00FEF		
G17	G416	h01000			h01001			h01002			h01003			· · · · ·	h010EC			h010ED			h010EE			h010EF		
G18	G415	h01100			h01101			h01102			h01103			· · · · ·	h011EC			h011ED			h011EE			h011EF		
G19	G414	h01200			h01201			h01202			h01203			· · · · ·	h012EC			h012ED			h012EE			h012EF		
G20	G413	h01300			h01301			h01302			h01303			· · · · ·	h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G417	G16	h1A000			h1A001			h1A002			h1A003			· · · · ·	h1A0EC			h1A0ED			h1A0EE			h1A0EF		
G418	G15	h1A100			h1A101			h1A102			h1A103			· · · · ·	h1A1EC			h1A1ED			h1A1EE			h1A1EF		
G419	G14	h1A200			h1A201			h1A202			h1A203			· · · · ·	h1A2EC			h1A2ED			h1A2EE			h1A2EF		
G420	G13	h1A300			h1A301			h1A302			h1A303			· · · · ·	h1A3EC			h1A3ED			h1A3EE			h1A3EF		
G421	G12	h1A400			h1A401			h1A402			h1A403			· · · · ·	h1A4EC			h1A4ED			h1A4EE			h1A4EF		
G422	G11	h1A500			h1A501			h1A502			h1A503			· · · · ·	h1A5EC			h1A5ED			h1A5EE			h1A5EF		
G423	G10	h1A600			h1A601			h1A602			h1A603			· · · · ·	h1A6EC			h1A6ED			h1A6EE			h1A6EF		
G424	G9	h1A700			h1A701			h1A702			h1A703			· · · · ·	h1A7EC			h1A7ED			h1A7EE			h1A7EF		
G425	G8	h1A800			h1A801			h1A802			h1A803			· · · · ·	h1A8EC			h1A8ED			h1A8EE			h1A8EF		
G426	G7	h1A900			h1A901			h1A902			h1A903			· · · · ·	h1A9EC			h1A9ED			h1A9EE			h1A9EF		
G427	G6	h1AA00			h1AA01			h1AA02			h1AA03			· · · · ·	h1AAEC			h1AAED			h1AAEE			h1AAEF		
G428	G5	h1AB00			h1AB01			h1AB02			h1AB03			· · · · ·	h1ABEC			h1ABED			h1ABEE			h1ABEF		
G429	G4	h1AC00			h1AC01			h1AC02			h1AC03			· · · · ·	h1ACEC			h1ACED			h1ACEE			h1ACEF		
G430	G3	h1AD00			h1AD01			h1AD02			h1AD03			· · · · ·	h1ADEC			h1ADED			h1ADEE			h1ADEF		
G431	G2	h1AE00			h1AE01			h1AE02			h1AE03			· · · · ·	h1AEEC			h1AEED			h1AEEE			h1AEEF		
G432	G1	h1AF00			h1AF01			h1AF02			h1AF03			· · · · ·	h1AFEC			h1AFED			h1AFEE			h1AFEF		

Instruction

Outline

The R61509 adopts 18-bit bus architecture in order to interface to high-performance microcomputer in high speed. The R61509 starts internal processing after storing control information (18, 16, 9, 8, 1 bit(s)), sent from the microcomputer, in the instruction register (IR) and the data register (DR). Since the internal operation of the R61509 is controlled by the signals sent from the microcomputer, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 ~ IB0) are called instruction. The following are the kinds of instruction of the R61509.

1. Specify index
2. Display control
3. Power management control
4. Set internal GRAM addresssss
5. Transfer data to and from the internal GRAM
6. Window address control
7. γ-correction
8. Panel Display Control

Normally, the instruction to write data is used the most often. The internal GRAM address is updated automatically as data is written to the internal GRAM, which, in combination with the window address function, contributes to minimizing data transfer and thereby lessens the load on the microcomputer. The R61509 writes instructions consecutively by executing the instruction within the cycle when it is written (instruction execution time: 0 cycle).

Instruction Data Format

As the following figure shows, the data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface.

The bits to which no instruction is assigned must be set to either “0” or “1” according to the following register tables. When changing only one instruction bit setting, the setting values in other bits in the register must be written.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	ID [10]	ID [9]	ID [8]	ID [7]	ID [6]	ID [5]	ID [4]	ID [3]	ID [2]	ID [1]	ID [0]

The index register specifies the indexes of control register or RAM control to be accessed. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

Display control

Device code read (R000h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0	0	1	0	1	0	1	0	0	0	0	1	0	0	1

The device code “1509”H is read out when reading out this register forcibly.

Driver Output Control (R001h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shift from S1 to S720.
When SS = “1”, the source driver output shift from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, RGB dots are assigned one to one from S1 to S720.
When SS = “1” and BGR = “1”, RGB dots are assigned one to one from S720 to S1.

When changing the SS and BGR bits, RAM data must be rewritten.

SM: Controls the scan mode in combination with GS setting. See “ Scan mode setting”.

LCD Driving Wave Control (R002h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	0	B/C [0]	0	0	0	0	0	0	NW [1]	NW [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B/C0: Selects the liquid crystal drive waveform VCOM. See "N-Line Inversion AC Drive" for details.

B/C = 0: frame inversion waveform is selected.
B/C = 1: line inversion waveform is selected.

NW[1:0]: Sets "n" for the number of lines from 1 to 4 to set the interval of inverting the polarity of line inversion drive (C-pattern waveform) when B/C0 = 1. The polarity is inverted at an interval of n + 1 lines.

Entry Mode (R003h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	TRI	DFM [0]	0	BGR	0	0	HWM	0	ORG	0	I/D [1]	I/D [0]	AM	0	EPF [1]	EPF [0]
Default value		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

The entry mode register includes instruction bits for setting how to write data from the microcomputer to the internal GRAM of the R61509.

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the R61509 writes data to the internal GRAM.

AM = "0", sets the horizontal direction.
AM = "1", sets the vertical direction.

When describing window address area, the data is written only within the area in the direction determined by I/D1-0, AM bits.

I/D[1:0]: Either increments (+1) or decrements (-1) the address counter (AC) automatically as the data is written to the GRAM. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]). The AM bit sets either horizontal or vertical direction in updating RAM address counter automatically when writing data to the internal RAM.

ORG: Moves the origin address according to the ID setting when a window address area is described. This function is enabled when writing data within the window address area using high-speed RAM write function.

ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.
ORG = 1: The origin address "h00000" is moved according to the I/D[1:0] setting.

Notes: 1. When ORG = 1, only the origin address "h00000" can be set in the RAM address set registers (R20h, R21h).
2. In RAM read operation, make sure to set ORG = 0.

HWM: The R61509 writes data in high speed with low power consumption by setting HWM = 1. The data to be written within the window address area is buffered in order to write the data in units of horizontal lines. This can minimize the number of RAM access and the power consumption required in data write operation.

When HWM = 1, make sure to set AM = 0 (horizontal direction) and write the data in each horizontal line of the window address area at a time. If the data is not enough to rewrite the horizontal line of the window address area, the GRAM data in that line is not overwritten.

Notes: 1. The R61509 requires no dummy write operation in high-speed write operation.
2. When terminating RAM data write operation in the middle of the line and executing another instruction, the data in the buffer is cleared.
3. When switching from high-speed RAM write operation to index write operation, wait at least 2 normal-write cycle periods (two t_{cycw} periods).

BGR: Reverses the order from RGB to BGR in writing 18-bit pixel data in the GRAM.

BGR = 0: Write data in the order of RGB to the GRAM.
BGR = 1: Reverse the order from RGB to BGR in writing data to the GRAM.

DFM[0]: In combination with the TRI setting, DFM sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM = 0 when not transferring data via 16-bit or 8-bit interface. DFM bit also specifies image data format (bpp) in MDDI operation. Set the bit in accordance with selected interface and image data format in RAM write operation.
DFM=0: 18bpp (R:G:B = 6:6:6), DFM=1: 16bpp (R:G:B = 5:6:5)

TRI: Selects the format to transfer data bits via 16-bit or 8-bit interface.

In 8-bit interface operation,
TRI = 0: 16-bit RAM data is transferred in two transfers.
TRI = 1: 18-bit RAM data is transferred in three transfers.

In 16-bit bus interface operation,
TRI = 0: 16-bit RAM data is transferred in one transfer.
TRI = 1: 18-bit RAM data is transferred in two transfers.

Make sure TRI = 0 when not transferring data via 16-bit or 8-bit interface. Also, set TRI = 0 during read operation.

EPF [1:0]: Set data format when 16bpp(R, G and B) to 18 bpp (r, g and b) is stored in internal RAM. EFP settings are effective when:
1. 80-system 16-bit interface, TRI=0
2. 80-system 8-bit interface, TRI=0
3. MDDI, DFM=1

Table 14

EPF	Expand 16bpp(R, G, B) to 18bpp(r, g, b)
2'h0	Same value as MSB is inputted to LSB of R and B r[5:0]={ R[4:0], R[4] } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], B[4] }
2'h1	"0" is inputted to LSB of r and b r[5:0]={ R[4:0], 1'h0 } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], 1'h0 } Except, R[4:0], B[4:0]=5'h1F → r, b[5:0]=6'h3F G[5:0]=6'h3F → g[5:0]=6'h3F
2'h2	"1" is inputted to LSB of r and b r[5:0]={ R[4:0], 1'h1 } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], 1'h1 } Except, R[4:0], B[4:0]=5'h0 → r, b[5:0]=6'h00 G[5:0]=6'h0 → g[5:0]=6'h00
2'h3	Setting disabled.

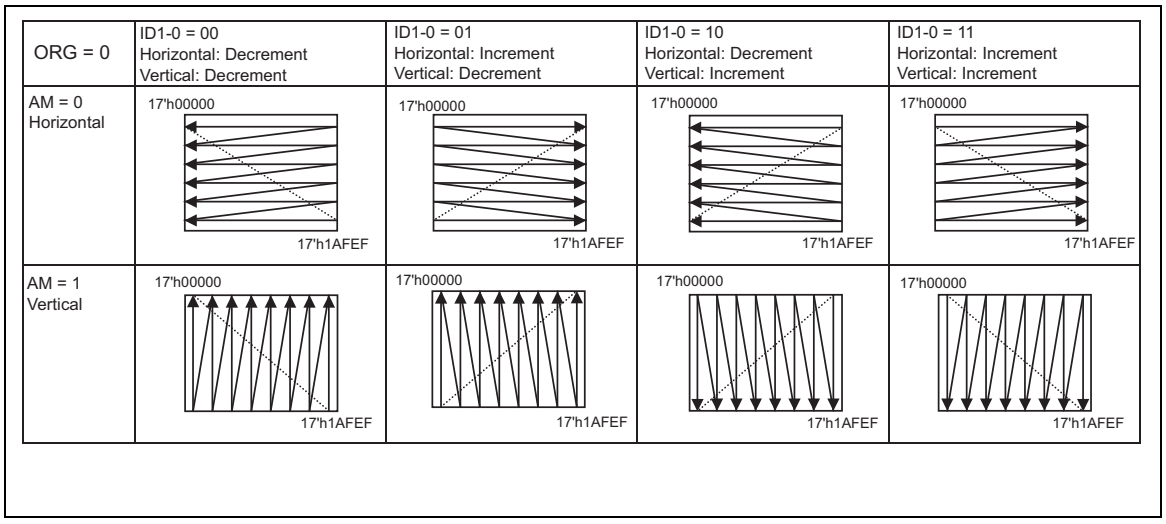


Figure 4 Automatic Address Update (ORG = 0, AM, ID)

Note: When writing data within the window address area with ORG = 0, any address within the window address area can be set as the starting point of data write operation.

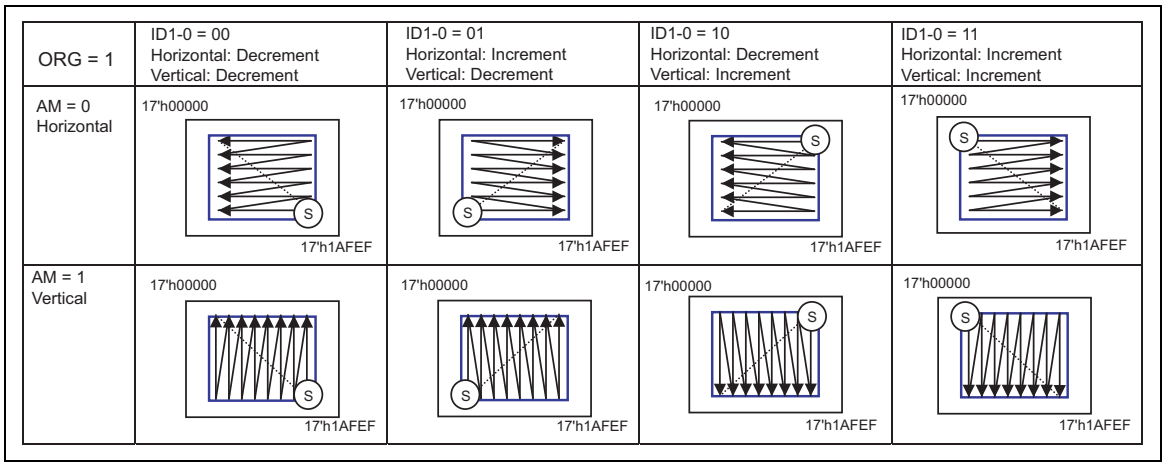


Figure 5 Automatic Address Update (ORG = 1, AM, ID)

Notes: 1. When ORG = 1, the address to start data write operation within the window address area is set at either corner of the window address area (the positions of the "S" in the circle in the above figure).

2. When ORG = 1, make sure to set the address "h00000" in the RAM address set register. Setting other addresses is prohibited.

Outline Sharpening Control (R006h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	EGMODE	0	0	0	0	0	AVST[2]	AVST[1]	AVST[0]	ADST[2]	ADST[1]	ADST[0]	DTHU[1]	DTHU[0]	DTHL[1]	DTHL[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EGMODE: Sets outline sharpening mode when EGMODE=1. When outline sharpening mode is set, data is written to internal RAM according to outline sharpening process. See "Outline Sharpening Function" for detail.

AVST[2:0]: Set coefficients used for smoothing edges between neighboring pixels. (Default: 3h'00)

AVST[2:0]	Coefficients
3'h00	0.125(=1/8)
3'h01	0.250(=2/8)
3'h02	0.375(=3/8)
3'h03	0.500(=4/8)
3'h04	0.625(=5/8)
3'h05	0.750(=6/8)
3'h06	0.875(=7/8)
3'h07	1.000(=8/8)

ADST[2:0]: Set the added coefficient in outline sharpening operation . (Default: 3h'00)

ADST[2:0]	Added coefficients
3'h00	0.0(Off)
3'h01	0.5(=1/2)
3'h02	1.0(=2/2)
3'h03	1.5(=3/2)
3'h04	2.0(=4/2)
3'h05	2.5(=5/2)
3'h06	3.0(=6/2)
3'h07	3.5(=7/2)

DTHU [1:0]: Sets the higher threshold of the brightness band of the object on which edge enhancement is performed . (Default: 2h'00)

DTHU[1:0]	Higher threshold
2'h00	15
2'h01	31
2'h02	47
2'h03	63

DTHL[1:0]: Sets the lower threshold of the brightness band of the object on which edge enhancement is performed. (Default: 2h'00)

DTHL[1:0]	Lower threshold
2'h00	0
2'h01	Setting disabled
2'h02	1
2'h03	2

Display Control 1 (R007h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	PTDE[1]	PTDE[0]	0	0	0	BASEE0	0	VON	GON	DTE	0	0	D[1]	D[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0]: A graphics display is turned on when writing D1 = "1", and is turned off when writing D1 = "0". When writing D1 = "0", the graphics display data is retained in the internal GRAM and the R61509 displays the data when writing D1 = "1". When D1 = "0", i.e. while no picture is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D1-0 = 2'b01, the R61509 continues internal display operation. When the display is turned off by setting D1-0 = 2'b00, the R61509's internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF. For details, see Instruction Setting for details.

Table 15

D[1:0]	BASEE	Source Output (S1-S720)	FMARK Signal	Internal Operation
2'h0	*	GND	Halt	Halt
2'h1	*	GND	Operation	Operation
2'h2	*	Non-lit display	Operation	Operation
2'h3	0	Non-lit display	Operation	Operation
	1	Base-image display	Operation	Operation

Notes: 1. The data write operation from microcomputer is not affected by the D[1:0] setting.
2. The non-lit display level is determined by NDL0 setting.

DTE, GON control the gate output level from G1 to G432 as follows.

Table 16

APE	GON	DTE	G1 ~ G432 Output Level
0	*	*	VGL (= GND)
1	0	0	VGH
	0	1	VGH
	1	0	VGL
	1	1	VGH/VGL

VON: Start VCOM output when VON=1. VCOM amplitude is decided by combination of VCON and VCOMG bits settings.

Table 17

APE	AP[2:0]	VON	VCOMG	VCOM Output
0	*	*	*	GND
1	0	0	0	GND
		0	1	Setting Disabled
		1	0	Setting Disabled
		1	1	Setting Disabled
	Other than 0	0	0	GND
		0	1	GND
		1	0	Amplitude=VCOMH-GND
		1	1	Amplitude=VCOMH-VCOML

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The R61509 drives the LCD at non-lit display level or displays only partial images.

BASEE = 1: A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

PTDE0: Partial display 1 enable bit.
PTDE1: Partial display 2 enable bit..

When PTDE0/1 = 0, partial display is turned off. Only a base image is displayed on the screen. When PTDE0/1 = 1, partial image is displayed. Set BASEE = 0 to turn off the base image.

Display Control 2 (R008h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0	0	0	0	FP [3]	FP [2]	FP [1]	FP [0]	0	0	0	0	BP [3]	BP [2]	BP [1]	BP [0]
Default value		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP[3:0]: Sets the number of lines for front porch period (a blank period made after the end of display).

BP[3:0]: Sets the number of lines for back porch period (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. After the front porch period, a blank period continues until next VSYNC input is detected.

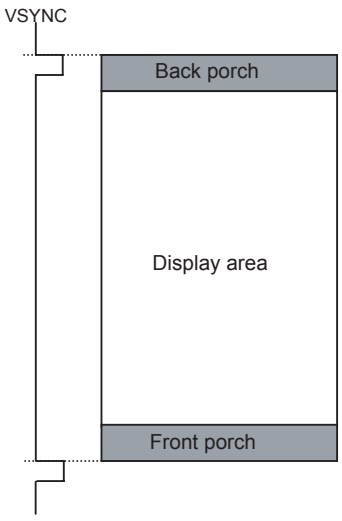
Note on Setting BP and FP:
Set the BP and FP bits as follows in the following operation modes, respectively.

Table 18

Internal clock operation mode	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines
RGB interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Table 19

FP[3:0] BP[3:0]	Front and Back Porch Period (Line Periods)
4'h0	Setting inhibited
4'h1	Setting inhibited
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
4'h5	5 lines
4'h6	6 lines
4'h7	7 lines
4'h8	8 lines
4'h9	9 lines
4'hA	10 lines
4'hB	11 lines
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting inhibited



Note: The output timing to the LCD panel is delayed by two line periods from the synchronous signal (VSYNC) input timing.

Figure 6 Front and Back Porch Periods

Display Control 3 (R009h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	PTV	PTS [2]	PTS [1]	PTS [0]	0	0	PTG [1]	PTG [0]	ISC [3]	ISC [2]	ISC [1]	ISC [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ISC[3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-lit display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 15. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 20

ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz
4'h0	Setting disabled	-
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8-F	Setting disabled	-

PTG[1:0]: Sets the scan mode in non-lit display area. Select frame-inversion AC drive when interval-scan is selected.

Table 21

PTG[1:0]	Scan mode in non-lit display area
2'h0	Normal scan
2'h1	Setting disabled
2'h2	Interval scan
2'h3	Setting disabled

PTS[2:0]: Sets the source output level in non-lit display area drive period. When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V31 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 22

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3'h0	V31	V0	V0 to V31	Register setting (DC0, DC1)
3'h1-3	Setting inhibited	Setting inhibited	-	-
3'h4	V31	V0	V0 and V31	1/2 the frequency set by DC0, DC1
3'h5-7	Setting inhibited	Setting inhibited	-	-

Notes: 1. The gate output level in non-display drive period is controlled by the PTG setting (off-scan mode).
2. The power efficiency improved by halting grayscale amplifiers and slowing down the step-up clock frequency can be obtained in non-display drive period.

PTV: Sets the VCOM output in non-lit display area drive period. The VCOM operation is halted by setting PTV = 1 in n-line inversion.

Table 23

PTV	VCOM operation in non-lit display drive period
0	Normal operation
1	Halts VCOM operation

Low Power Control (R00Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0	0	0	0	0	0	0	0	0	0	0	VEM [0]	0	0	0	COL
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

COL: When COL = 1, the R61509 enters the eight-color display mode. RAM data rewrite operation is not required when setting the eight-color display mode. Set the 8-color mode instruction according to the 8-color mode sequence.

The electrical potential of liquid crystal drive in 8-color display mode is V0/V31.

Table 24

COL	Display Color
1'h0	262,144 colors
1'h 1	8 colors

VEM[0]: VCOM equalize switch.

When VEM[0]=1, VCOMH first drops to GND and then VCOML. (VCOMH → GND → VCOML). This is to reduce power consumption in VCOM drive.

Make sure that VCI < VCOMH and GND > VCOML when this function is used.

Check the picture quality and effect on the panel before using this low-power consumption VCOM function.

External Display Interface Control 1 (R00Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	ENC [2]	ENC [1]	ENC [0]	0	0	0	RM	0	0	DM [1]	DM [0]	0	0	RIM [1]	RIM [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets the interface format when RGB interface is selected by RM and DM bits. Set RIM[1:0] bits before starting display operation via RGB interface. Do not change the setting while the R61509 performs display operation.

Table 25

RIM[1:0]	RGB Interface operation	Colors
2'h0	18-bit RGB interface (1 transfer/pixel) via DB17-0	262,144
2'h1	16-bit RGB interface (1 transfer/pixel) via DB17-13 and DB11-1	65,536
2'h2	6-bit RGB interface (3 transfers/pixel) via DB17-12	262,144
2'h3	Setting inhibited	-

Notes: 1: Instruction bits are set via system interface.
2: Transfer the RGB dot data one by one in synchronization with DOTCLK in 6-bit RGB interface operation.

DM[1:0]: The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

Table 26 Display Interface

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting inhibited

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

Table 27 RAM Access Interface

RM	RAM Access Interface
0	System interface/VSYNC interface
1	RGB interface

ENC[2:0]: Sets the RAM write cycle via RGB interface.

Table 28

ENC[2:0]	RAM Write Cycle (frame periods)
3'h0	1 frame
3'h1	2 frames
3'h2	3 frames
3'h3	4 frames
3'h4	5 frames
3'h5	6 frames
3'h6	7 frames
3'h7	8 frames

External Display Interface Control 2 (R00Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of DOTCLK pin.

DPL = 0: input data on the rising edge of DOTCLK
DPL = 1: input data on the falling edge of DOTCLK

EPL: Sets the signal polarity of ENABLE pin.

EPL = 0: writes data DB17-0 when ENABLE = "0" and disables data write operation when ENABLE = "1".
EPL = 1: writes data DB17-0 when ENABLE = "1" and disables data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of HSYNC pin.

HSPL = 0: low active
HSPL = 1: high active

VSPL: Sets the signal polarity of VSYNC pin.

VSPL = 0: low active
VSPL = 1: high active

Panel Interface Control 1 (R010h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0	0	0	0	0	0	DIVI [1]	DIVI [0]	0	0	0	RTNI [4]	RTNI [3]	RTNI [2]	RTNI [1]	RTNI [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

RTNI[4:0]: Sets 1H (line) period. This setting is valid when the R61509's display operation is synchronized with internal clock signal.

Table 29 Clocks per Line (Internal Clock Operation)

RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line
5'h00-5'h0F	Setting inhibited	5'h18	24 clocks
5'h10	16 clocks	5'h19	25 clocks
5'h11	17 clocks	5'h1A	26 clocks
5'h12	18 clocks	5'h1B	27 clocks
5'h13	19 clocks	5'h1C	28 clocks
5'h14	20 clocks	5'h1D	29 clocks
5'h15	21 clocks	5'h1E	30 clocks
5'h16	22 clocks	5'h1F	31 clocks
5'h17	23 clocks		

Note: In Power Supply Instruction Setting, Deep Standby Exit Sequence and Sleep Mode Exit Sequence, RTNI bit must be set at the "Initial instruction setting" state. See Power Supply Instruction Setting and Shutdown Mode IN/EXIT Sequences for detail of the timing to set the bit.

DIVI[1:0]: Sets the division ratio of the internal clock frequency. The R61509's internal operation is synchronized with the frequency divided internal clock, which is set according to the division ratio determined by DIVI[1:0] setting. The frame frequency can be changed by setting RTNI and DIVI bits. When changing the number of lines to drive the LCD panel, adjust the frame frequency too. For details, see Frame-Frequency Adjustment Function. In RGB interface operation, the DIVI[1:0] setting has no effect.

Table 30 Division Ratio (Internal Operation)

DIVI[1:0]	Division Ratio	Internal Operation Clock Unit
2'h0	1/1	1 x OSC
2'h1	1/2	2 x OSC
2'h2	1/4	4 x OSC
2'h3	1/8	8 x OSC

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{fosc}{\text{Clocks per line x division ratio x (line + BP + FP)}} \; [Hz]$$

fosc : RC oscillation frequency
Line: Number of lines to drive the LCD (NL bits)
Division ratio: DIVI
Clocks per line: RTNI

Panel Interface Control 2 (R011h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	SDTI[2]	SDTI[1]	SDTI[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled when the R61509's display operation is synchronized with internal clock signals.

Table 31

NOWI[2:0]	Non-overlap period	NOWI[2:0]	Non-overlap period
3'h0	0 (internal clock *see note)	3'h4	4 (internal clock *see note)
3'h1	1	3'h5	5
3'h2	2	3'h6	6
3'h3	3	3'h7	7

Note: The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits.

SDTI[2:0]: Sets the source output delay period from the reference point. For the relationships between gate interface signals, see Liquid Crystal Panel Interface Timing.

Table 32

SDTI[2:0]	Source output delay period
3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Notes: 1. The number of clocks in the table setting is measured from the reference point.
2. 1 clock = (internal oscillation clock (OSC1) period) x (division ratio)
3. The reference point is where SFTCLK rises when the rising position is set to 0 clock.

Panel Interface Control 3 (R012h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	VEQ WI[1]	VEQ WI[0]	0	0	0	0	0	SEQ WI[2]	SEQ WI[1]	SEQ WI[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VEQWI[1:0]: Sets low power VCOM drive period. The setting is enabled when the R61509's display operation is synchronized with internal clock signals.

Table 33

VEQWI[1:0]	Low power VCOM drive period
2'h0	0 (internal clock *see note)
2'h1	1 clock
2'h2	2 clocks
2'h3	3 clocks

Note: The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits. The number of clocks is measured from the reference point. The reference point is the alternating position of VCOM, which is set by SDTI[2:0] bits.

SEQWI[2:0]: Sets source equalize period. SEQWI setting is enabled when the R61509 executes display operation in synchronization with internal clock.

Table 34

SEQWI[2:0]	Source Equalize Period
3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: The clock is the frequency divided clock, which is set by DIVI[[1:0] bits.

Panel Interface Control 4 (R020h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	DIVE [1]	DIVE [0]	0	RTNE [6]	RTNE [5]	RTNE [4]	RTNE [3]	RTNE [2]	RTNE [1]	RTNE [0]
Default		0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0

RTNE[6:0]: Sets RTNE in combination with DIVE to the number of DOTCLK included in 1H (1 line) period according to the following formula, when the R61509's display operation is synchronized with RGB interface signals.

DIVE (division ratio) x RTNE (DOTCLKs) ≤ DOTCLKs in 1H period.

Table 35 DOTCLKs in 1H period (RGB interface operation)

RTNE[6:0]	Clocks per line period (1H)	RTNE[6:0]	Clocks per line period (1H)	RTNE[6:0]	Clocks per line period (1H)	RTNE[6:0]	Clocks per line period (1H)
7'h00	Setting inhibited	7'h20	32 clocks	7'h40	64 clocks	7'h60	96 clocks
7'h01	Setting inhibited	7'h21	33 clocks	7'h41	65 clocks	7'h61	97 clocks
7'h02	Setting inhibited	7'h22	34 clocks	7'h42	66 clocks	7'h62	98 clocks
7'h03	Setting inhibited	7'h23	35 clocks	7'h43	67 clocks	7'h63	99 clocks
7'h04	Setting inhibited	7'h24	36 clocks	7'h44	68 clocks	7'h64	100 clocks
7'h05	Setting inhibited	7'h25	37 clocks	7'h45	69 clocks	7'h65	101 clocks
7'h06	Setting inhibited	7'h26	38 clocks	7'h46	70 clocks	7'h66	102 clocks
7'h07	Setting inhibited	7'h27	39 clocks	7'h47	71 clocks	7'h67	103 clocks
7'h08	Setting inhibited	7'h28	40 clocks	7'h48	72 clocks	7'h68	104 clocks
7'h09	Setting inhibited	7'h29	41 clocks	7'h49	73 clocks	7'h69	105 clocks
7'h0A	Setting inhibited	7'h2A	42 clocks	7'h4A	74 clocks	7'h6A	106 clocks
7'h0B	Setting inhibited	7'h2B	43 clocks	7'h4B	75 clocks	7'h6B	107 clocks
7'h0C	Setting inhibited	7'h2C	44 clocks	7'h4C	76 clocks	7'h6C	108 clocks
7'h0D	Setting inhibited	7'h2D	45 clocks	7'h4D	77 clocks	7'h6D	109 clocks
7'h0E	Setting inhibited	7'h2E	46 clocks	7'h4E	78 clocks	7'h6E	110 clocks
7'h0F	Setting inhibited	7'h2F	47 clocks	7'h4F	79 clocks	7'h6F	111 clocks
7'h10	16 clocks	7'h30	48 clocks	7'h50	80 clocks	7'h70	112 clocks
7'h11	17 clocks	7'h31	49 clocks	7'h51	81 clocks	7'h71	113 clocks
7'h12	18 clocks	7'h32	50 clocks	7'h52	82 clocks	7'h72	114 clocks
7'h13	19 clocks	7'h33	51 clocks	7'h53	83 clocks	7'h73	115 clocks
7'h14	20 clocks	7'h34	52 clocks	7'h54	84 clocks	7'h74	116 clocks
7'h15	21 clocks	7'h35	53 clocks	7'h55	85 clocks	7'h75	117 clocks
7'h16	22 clocks	7'h36	54 clocks	7'h56	86 clocks	7'h76	118 clocks
7'h17	23 clocks	7'h37	55 clocks	7'h57	87 clocks	7'h77	119 clocks
7'h18	24 clocks	7'h38	56 clocks	7'h58	88 clocks	7'h78	120 clocks
7'h19	25 clocks	7'h39	57 clocks	7'h59	89 clocks	7'h79	121 clocks
7'h1A	26 clocks	7'h3A	58 clocks	7'h5A	90 clocks	7'h3A	122 clocks
7'h1B	27 clocks	7'h3B	59 clocks	7'h5B	91 clocks	7'h7B	123 clocks
7'h1C	28 clocks	7'h3C	60 clocks	7'h5C	92 clocks	7'h7C	124 clocks
7'h1D	29 clocks	7'h3D	61 clocks	7'h5D	93 clocks	7'h7D	125 clocks
7'h1E	30 clocks	7'h3E	62 clocks	7'h5E	94 clocks	7'h7E	126 clocks
7'h1F	31 clocks	7'h3F	63 clocks	7'h5F	95 clocks	7'h7F	127 clocks

DIVE[1:0]: Sets the division ratio of DOTCLK. The R61509's internal operation is synchronized with the frequency-divided DOTCLK, the frequency of which is divided by the division ratio set by DIVE[1:0]. This setting is enabled while the R61509's display operation is synchronized with RGB interface signals.

Table 36 Division Ratio of DOTCLK (RGB interface operation)

DIVE[1:0]	Division Ratio	Internal operation clock unit in RGB interface operation			
		16-bit x 1 transfer RGB Interface	DOTCLK = 5MHz	6-bit x3 transfers RGB Interface	DOTCLK = 15MHz
2'h0	Setting inhibited	Setting inhibited	-	Setting inhibited	-
2'h1	1/4	4 DOTCLKs	0.8 μS	12 DOTCLKs	0.8 μS
2'h2	1/8	8 DOTCLKs	1.6 μS	24 DOTCLKs	1.6 μS
2'h3	1/16	16 DOTCLKs	3.2 μS	48 DOTCLKs	3.2 μS

Panel Interface Control 5 (R021h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	NOWE[3]	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	SDTE[3]	SDTE[2]	SDTE[1]	SDTE[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOWE[3:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled when the R61509's display operation is synchronized with internal clock signals.

Table 37

NOWE[3:0]	Non-overlap period	NOWE[3:0]	Non-overlap period
4'h0	0 (internal clock *see note)	4'h8	8
4'h1	1	4'h9	9
4'h2	2	4'hA	10
4'h3	3	4'hB	11
4'h4	4	4'hC	12
4'h5	5	4'hD	13
4'h6	6	4'hE	14
4'h7	7	4'hF	15

Note: 1 clock = (number of data transfer/pixel) x DIV (division ratio) [DOTCLK]

SDTE[3:0]: Sets the source output delay period from the reference point when the R61509's display operation is synchronized with DOTCLK (DM = 2'h1). For the relationships between gate interface signals and LTPS liquid crystal panel interface signals, see Liquid Crystal Panel Interface Timing.

Table 38

SDTE[3:0]	Source output delay period	SDTE[3:0]	Source output delay period
4'h0	0 clocks	4'h8	8 clocks
4'h1	1 clock	4'h9	9 clocks
4'h2	2 clocks	4'hA	10 clocks
4'h3	3 clocks	4'hB	11 clocks
4'h4	4 clocks	4'hC	12 clocks
4'h5	5 clocks	4'hD	13 clocks
4'h6	6 clocks	4'hE	14 clocks
4'h7	7 clocks	4'hF	15 clocks

Notes: 1. The number of clocks in the table setting is measured from the reference point.
2. 1 clock = (DOTCLK period) x (division ratio)
3. The reference point is falling edge of gate control signals.

Panel Interface Control 6 (R022h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	VEQ WE [2]	VEQ WE [1]	VEQ WE [0]	0	0	0	0	SEQ WE [3]	SEQ WE [2]	SEQ WE [1]	SEQ WE [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VEQWE[2:0]: Sets low power VCOM drive period. The setting is enabled when the R61509's display operation is synchronized with RGB interface signals.

Table 39

VEQWE[2:0]	Source output delay period	VEQWE[2:0]	Source output delay period
3'h0	0 clocks (*see Notes)	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Notes: 1. 1 clock = (number of data transfer/pixel) x DIV (division ratio) [DOTCLK]

2. The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits. The number of clocks is measured from the reference point. The reference point is the alternating position of VCOM, which is set by SDTE[3:0] bits.

SEQWE[2:0]: Sets source equalize period. SEQWE setting is enabled when the R61509 executes display operation via RGB interface.

Table 40

SEQWE[3:0]	Source Equalize Period	SEQWE[3:0]	Source Equalize Period
4'h0	0 clocks	4'h8	8 clocks
4'h1	1 clock	4'h9	9 clocks
4'h2	2 clocks	4'hA	10 clocks
4'h3	3 clocks	4'hB	11 clocks
4'h4	4 clocks	4'hC	12 clocks
4'h5	5 clocks	4'hD	13 clocks
4'h6	6 clocks	4'hE	14 clocks
4'h7	7 clocks	4'hF	15 clocks

Note: 1 clock = (number of data transfer/pixel) x DIV (division ratio) [DOTCLK]

Frame Marker Control (R090h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	FMKM	FMI [2]	FMI [1]	FMI [0]	0	0	0	FMP [8]	FMP [7]	FMP [6]	FMP [5]	FMP [4]	FMP [3]	FMP [2]	FMP [1]	FMP [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0]: Sets the output position of frame synchronous signal (frame marker). A pulse (FMARK) is output by starting from back porch during a 1H period when FMP[8:0] = 9'h000 (high active, amplitude: IOVCC1-GND). FMP[8:0] is used as a trigger signal for write operation in synchronization with frame.

Setting range: 9'h000 ≤ FMP ≤ BP + NL + FP - 1

For details, see MDDI-FMARK Interface.

Table 41

FMP[8:0]	FMARK output position
9'h000	0
9'h001	1
9'h002	2
	:
9'h1BD	445
9'h1BE	446
9'h1BF	447

FMI[2:0]: Sets FMARK output interval by FMI register setting according to the update period of display data and transfer rate. Set FMARK = 1 in timing output from FMARK pin.

Table 42

FMI[2]	FMI[1]	FMI[0]	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting inhibited

FMKM: Output from FMARK pin by connecting FLM signal to TSC pin output from the sub display in MDDI sub display operation. Used as frame synchronous signal for moving picture display on the sub display in MDDI operation.

Table 43

FMKM	FMARK pin output
1'h0	R61509's frame signal
1'h1	Sub display frame signal (TSC pin connect signal)

Notes 1 FMKM cannot be used in shut down mode.

2 The R61509's display operation is not related to TSC input signal when FMKM = 1. FMP and

FMI settings are disabled when FMKM = 1.

MDDI Sub-display Control (R092h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SIM [1]	SIM [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SIM[1:0]: Sets data format to transfer data to subdisplay when MDDI sub-display interface is chosen. SIM [1:0] setting and format of video stream packet should be decided following subdisplay data format. See "MDDI Sub-Display Interface" for detail.

SIM[1:0]	Sub display interface data format	Video Stream Packet
2'b00	I80 system, 18bit, one-transfer	18bpp
2'b01	Setting Disabled	-
2'b10	I80 system, 16bit, one transfer	16bpp
2'b11	Setting Disabled	-

Power Control

Power Control 1 (R100h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	SAP [1]	SAP [0]	SAP	0	BT [2]	BT [1]	BT [0]	APE	AP [2]	AP [1]	AP [0]	0	DSTB	SLP	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP: When SLP = 1, the R61509 enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change to the GRAM data and instruction setting is accepted and the GRAM data and the instruction settings are maintained in sleep mode.

DSTB: When DSTB = 1, the R61509 enters the shut down mode. In shut down mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the R61509 is in the shut down mode. Set the instruction again after exiting the shut down mode. GND level is outputted to the panel in the shut down mode.

AP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current, the better the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0]=3'h0 to reduce power consumption. Set AP[2:0]=3'h7 and SAP[1:0]=2'h3 when VC is not 3'h7.

Table 44 Constant Current in Operational Amplifiers

AP[2:0]	**In LCD drive power supply amplifiers**	**In grayscale voltage amplifiers**
3'h0 (Note 1)	Halt operational amplifiers and step-up circuits	Halt
3'h1 (Note 1)	0.5	0.62
3'h2 (Note 1)	0.75	0.71
3'h3 (Note 1)	1	1
3'h4-6	Setting inhibited	Setting inhibited
3'h7 (Note 2)	1.6	1

The values in the table represent the ratios of currents in respective settings to the current when AP[2:0]=3'h3.

Note 1: Set SAP[1:0]=2'h0 when AP[2:0]=3'h0, 3'h1, 3'h2, 3'h3.

Note 2: Set SAP[1:0]=2'h3 when AP[2:0]=3'h7.

APE: Liquid crystal power supply enable bit. Set APE = "1" when starting the generation of liquid crystal power supply according to the liquid crystal power supply startup sequence.

Table 45

APE	Liquid crystal power supply circuit	Grayscale voltage generating circuit
1'h0	Halt	Halt
1'h1	Operate	Operate

SAP: When SAP = "0", the internal source output circuit is halted (S1-S720 = GND). When SAP = "1", grayscale voltages are output from the source output circuit. Set SAP = "0" when turning on the power supply such as liquid crystal power supply circuit. After starting up the power supply circuit, set SAP = "1".

SAP[1:0]: Adjusts constant current in the grayscale voltage generating circuit .

Set SAP[1:0]=2'h3 when AP[2:0]=3'h7. Power consumption in the source driver unit is reduced.
Set SAP[1:0]=2'h0 when AP[2:0]=3'h0-3. Constant current in the operational amplifiers is set by AP[2:0] bit.

BT[2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

Table 46 Step-Up Factor for Step-Up Circuits 1/2

<table>
<tr><th>BT[2:0]</th><th>DDVDH</th><th>VCL</th><th>VGH</th><th>VGL</th><th>Capacitor Connection Pins</th></tr>
<tr><td>3'h1-2</td><td>Setting Disabled</td><td>Setting Disabled</td><td>Setting Disabled</td><td>Setting Disabled</td><td>Setting Disabled</td></tr>
<tr><td>3'h0</td><td rowspan="7">VCI1×2
[x 2]</td><td rowspan="7">-VCI1
[x -1]</td><td>DDVDH×3
[x 6]</td><td>-(VCI1+DDVDH×2)
[x –5]</td><td>VLOUT1, VLOUT2, VLOUT3, VLOUT4,
C11±, C12±, C13±,
C21±,C22± (Note 4)</td></tr>
<tr><td>3'h3</td><td rowspan="3">VCI1+DDVDH×3
[x 7]</td><td>-(VCI1+DDVDH×2)
[x –5]</td><td rowspan="3">VLOUT1, VLOUT2, VLOUT3, VLOUT4,
C11±, C12±, C13±,
C21±,C22±,C23±</td></tr>
<tr><td>3'h4</td><td>-(DDVDH×2)
[x –4]</td></tr>
<tr><td>3'h5</td><td>-(VCI1+DDVDH)
[x –3]</td></tr>
<tr><td>3'h6</td><td rowspan="2">DDVDH×3
[x 6]</td><td>-(DDVDH×2)
[x -4]</td><td rowspan="2">VLOUT1, VLOUT2, VLOUT3, VLOUT4,
C11±, C12±, C13±,
C21±,C22± (Note 4)</td></tr>
<tr><td>3'h7</td><td>-(VCI1+DDVDH)
[x –3]</td></tr>
</table>

Notes: 1. The factors in the brackets show the step-up factors from VCI1.
2. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL levels.
3. Make sure DDVDH = max. 6.0V, VGH = max. 17.5V, VGL = min. -12.5V and VCL = max-3.0V.
4. C23± pins may not be connected in particular VGH output settings.

Power Control 2 (R101h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	DC1 [2]	DC1 [1]	DC1 [0]	0	DC0 [2]	DC0 [1]	DC0 [0]	0	VC [2]	VC [1]	VC [0]
Default value		0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0

Table 47 Step-up Frequency (Step-up Circuit 1)

DC0[2:0]	Step-up circuit 1: step-up frequency (f_{DCDC1})
3'h0	F_{DCDC}
3'h1	f_{DCDC} / 2
3'h2	f_{DCDC} / 4
3'h3	f_{DCDC} / 8
3'h4	f_{DCDC} / 16
3'h5	Setting inhibited
3'h6	Halt Step-up circuit 1
3'h7	Setting inhibited

Note 1: Make sure the DC0, DC1 setting restriction: $f_{DCDC1} \geq f_{DCDC2}$.

Note 2: $=f_{DCDC}$ =f_{OSC} （when DCM=0）

Table 48 Step-up Frequency (Step-up Circuit 2)

DC1[2:0]	Step-up circuit 2: step-up frequency (f_{DCDC2})
3'h0	f_{DCDC} / 16
3'h1	f_{DCDC} / 32
3'h2	f_{DCDC} / 64
3'h3	f_{DCDC} / 128
3'h4	f_{DCDC} / 256
3'h5	Setting inhibited
3'h6	Halt Step-up circuit 2
3'h7	Setting inhibited

Table 49 VCIOUT output level (Note 4)

VC[2:0]	VCIOUT (Reference Voltage) (VCI1 Voltage)	
3'h0	0.94 x VCILVL	
3'h1	0.89 x VCILVL	
3'h2	Setting inhibited	
3'h3	Setting inhibited	
3'h4	0.76 x VCILVL	Note 3
3'h5	Setting inhibited	
3'h6	0.70 x VCILVL	Note 3
3'h7	1.00 x VCILVL	

Note 3: VC=3'h4 and 4'h6 are allowed to set only during the power ON sequence. The setting is inhibited during normal display operation.

Note 4: VC = 3'h7 is recommended. When VC≠3'h7, set AP[2:0]=3'h7 and SAP[1:0]=2'h3.

Power Control3 (R102h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	0	VCMR0[0]	VREG1R	0	PSON	PON	VRH [3]	VRH [2]	VRH [1]	VRH [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PON: Controls the operation to generate VLOUT3. In setting the PON bit, follows the power-supply startup sequence.

PON = 0: Halts the step-up operation to generate VLOUT3.
PON = 1: Starts the step-up operation to generate VLOUT3.

PSON: Power supply ON bit. When turning on the power supply, set PSE = 1 first and then set PSON = 1 to start internal power supply operation.

VREG1R: Selects VREG1OUT generating reference voltage.

Table 50

VREG1R	VREG1OUT generating reference voltage
0	VCILVL (External)
1	VCIR (Internal reference voltage)

VCMR0[0]: Selects either external resistance (VCOMR pin) or internal electronic volume (VCM[4:0]) to set the electrical potential of VCOMH. The internal electronic volume can be set by VCM bits

Table 51

VCMR0[0]	VCOMH Electrical Potential setting
0	VCOMR
1	Internal electronic volume

VRH[3:0]: Sets the factor to generate VREG1OUT from VCILVL.

Table 52 VREG1OUT

VRH	VREG1OUTvoltage (External reference voltage VCILVL)	VREG1OUT voltage (Internal reference voltageVCIR)
4'h0-4'h3	Halt (Hiz)	Halt (Hiz)
4'h4-4'h7	Setting Disabled	Setting Disabled
4'h8	VCILVL×1.60	2.5V×1.60 = 4.00V
4'h9	VCILVL×1.65	2.5V×1.65 = 4.13V
4'hA	VCILVL×1.70	2.5V×1.70 = 4.25V
4'hB	VCILVL×1.75	2.5V×1.75 = 4.38V
4'hC	VCILVL×1.80	2.5V×1.80 = 4.50V
4'hD	VCILVL×1.85	2.5V×1.85 = 4.63V
4'hE	VCILVL×1.90	2.5V×1.90 = 4.75V
4'hF	Setting Disabled	Setting Disabled

Note 1: Adjust the VC and VRH settings so that VREG1OUT ≤ (DDVDH-0.5)V.
Note 2: VCIR is internally generated voltage. Design value: 2.5V.

Power Control 4 (R103h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	VCOMG	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0]: Selects the factor of VREG1OUT to set the amplitude of VCOM alternating voltage from 0.70 to 1.24.

Table 53

VDV[4:0]	Vcom amplitude (VCS)	VDV[4:0]	Vcom amplitude (VCS)
5'h0	VREG1OUT x 0.70	5'h10	VREG1OUT x 1.02
5'h1	VREG1OUT x 0.72	5'h11	VREG1OUT x 1.04
5'h2	VREG1OUT x 0.74	5'h12	VREG1OUT x 1.06
5'h3	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.08
5'h4	VREG1OUT x 0.78	5'h14	VREG1OUT x 1.10
5'h5	VREG1OUT x 0.80	5'h15	VREG1OUT x 1.12
5'h6	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.14
5'h7	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.16
5'h8	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.18
5'h9	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.20
5'hA	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.22
5'hB	VREG1OUT x 0.82	5'h1B	VREG1OUT x 1.24
5'hC	VREG1OUT x 0.94	5'h1C	Setting disabled
5'hD	VREG1OUT x 0.96	5'h1D	Setting disabled
5'hE	VREG1OUT x 0.98	5'h1E	Setting disabled
5'hF	VREG1OUT x 1.00	5'h1F	Setting disabled

Note 1: Set VDV[3:0] so that VCOM amplitude becomes 6.0V or less.

Note 2: Set VCOML (VCOMH-VCOM amplitude) ≤ 0V.

VCOMG: Sets VCOML output level.

VCOMG = 0: VCOML output is fixed to GND. The VDV[4:0] setting is disabled. VCOML output or VCL output is halted.

VCOMG = 1: VCOML output at Low is fixed to VCOML. VCOML output voltage is set by the VDV[4:0] setting.

Table 54

APE	AP[2:0]	VON	VCOMG	VCOM Output
0	*	*	*	GND
1	0	0	0	GND
		0	1	Setting disabled
		1	0	Setting disabled
		1	1	Setting disabled
	Other than 0	0	0	GND
		0	1	GND
		1	0	Amplitude=VCOMH-GND
		1	1	Amplitude=VCOMH-VCOML

Power consumption can be reduced by halting VCOML generating circuit and VCL voltage when VCOML = 0 (VCL capacitance is not required). Whether this setting is enabled or not depends on liquid crystal panel characteristics, when VCOML = GND.

Power Control 5 (R107h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	0	0	0	0	DCM [1]	DCM [0]	DCT [3]	DCT [2]	DCT [1]	DCT [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DCT[3:0]: Sets the synchronizing timing of the step-up reference clock for display operation in 1H period.

Table 55

DCT[3:0]	Reference clock for step-up operation (DCDC1) Synchronizing timing for display operation
4'h0	0 clock
4'h1	1 clock
4'h2	2 clocks
4'h3	3 clocks
4'h4	4 clocks
4'h5	5 clocks
4'h6	6 clocks
4'h7	7 clocks
4’h8	8 clocks
4’h9	9 clocks
4’hA	10 clocks
4’hB	11 clocks
4’hC	12 clocks
4’hD	13 clocks
4’hE	14 clocks
4’hF	15 clocks

Notes: 1. The DCT [3:0] setting is disabled when DCM = 0.

2. When the R61509’s operation is synchronized with internal clock signal, DIVI [1:0] (R010) sets reference clock for step-up operation.

3. When the R61509’s operation is synchronized with internal clock signal, namely it used RGB interface, RIM [1:0] (R00Ch) and DIVE [1:0] (R020h) set reference clock for step-up operation.

DCM[1:0]: Sets display synchronous display operation mode of step-up circuits.

Table 56

DCM[0] DCM[1]	Step-up circuit Display synchronous function	Reference clock for step-up operation	Step-up reference clock
1'h0	Invalid	OSC clock	-
1'h1	Step-up circuit 1: Horizontal synchronous Step-up circuit 2: Vertical synchronous	Display operation clock (including DOTCLK)	RTNI setting/1H (RTNE setting/1H)Note 2
2'h2	Invalid	Display operation clock (including DOTCLK)	16 clk / 1H
2'h3	Step-up circuit 1: Horizontal synchronous Step-up circuit 2: Vertical synchronous	Display operation clock (including DOTCLK)	16 clk / 1H

When DCM[0]=1, step-up operation of step-up circuit 1 is synchronized with display operation of every line.
At the same time, step-up operation of step-up circuit 2 is synchronized with display operation of every line.
When DCM[1]=1, step-up reference clock that generates every 1H period is set at 16 clocks.

Frequencies for step-up reference clock, fDCDC

When DCM＝0, f_{DCDC} ＝ f_{OSC}

When DCM≠0,

i) Display operation synchronized with internal clock

f_{DCDC} ＝ f_{OSC}×DIVI（division ratio）

ii)Display operation synchronized with external clock (RGB I/F), RTNE≤7'h1F

f_{DCDC} ＝ f_{DOTCLK}×（transfer times /pixel）×DIVE (division ratio)

iii) Display operation synchronized with external clock (RGB I/F), RTNE≥7'h20

f_{DCDC} ＝ f_{DOTCLK}×（transfer times/pixel）×DIVE（division ratio）×（div. 1/2）

Note 1: DC0 and DC1 set division ratio based on step-up reference clock set by DCM.

Note 2: When display operation is synchronized with external clock and RTNE≥7'h20, step-up reference clock becomes (clocks per line period set by RTNE bits÷2).

Power Control 6 (R110h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PSE: Power supply startup enable bit.

PSE = 1: The R61509's power supply is started by setting PSON when PSE =1. When completing the power supply generating operation, PSE is set to 0.

PSE = 0: Power supply sequencer is reset. When halting the operating power supply sequencer, set PSE = 0. When starting up power supply without power supply sequencer, set PSE = 0. The power sequencer enables the register settings sequentially at the designated timing and order.

Power Control 7 (R112h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	TBT [1]	TBT [0]	0	1	1	0	0	0	0	0
Default		0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0

TBT[1:0]: Sets position from where BT bit (R100h) is enabled by number of frame(s). Set TBT=2'h0 in Power Supply Instruction Setting, Deep Standby Exit Sequence and Sleep Mode Exit Sequence.

See Power supply Instruction Setting.

RAM Access

RAM Address Set (Horizontal Address) (R200h)
RAM Address Set (Vertical Address) (R201h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R200	R/W	1	0	0	0	0	0	0	0	0	AD [7]	AD [6]	AD [5]	AD [4]	AD [3]	AD [2]	AD [1]	AD [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R201	R/W	1	0	0	0	0	0	0	0	AD [16]	AD [15]	AD [14]	AD [13]	AD [12]	AD [11]	AD [10]	AD [9]	AD [8]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the R61509 writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM = "1"), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

Note 2: In internal clock operation and VSYNC interface operation (RM = "0"), the address AD16-0 is set when executing the instruction.

Table 57 GRAM Address setting range

AD[16:0]	GRAM Data Setting
17'h00000 – 17'h000EF	Bitmap data on the first line
17'h00100 – 17'h001EF	Bitmap data on the second line
17'h00200 – 17'h002EF	Bitmap data on the third line
17'h00300 – 17'h003EF	Bitmap data on the fourth line
17'h00400 – 17'h004EF	Bitmap data on the fifth line
:	:
17'h1AC00 – 17'h1ACEF	Bitmap data on the 429th line
17'h1AD00 – 17'h1ADEF	Bitmap data on the 430th line
17'h1AE00 – 17'h1AEEF	Bitmap data on the 431st line
17'h1AF00 – 17'h1AFEF	Bitmap data on the 432nd line

Write Data to GRAM (R202h)

R/W	RS	
W	1	RAM write data WD[17:0] is transferred via different data bus in different interface operation.
RGB interface		RAM write data WD[17:0] is transferred via different data bus in different interface operation.

WD[17:0]: The R61509 develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation.

The GRAM data represents the grayscale level. The R61509 automatically updates the address according to AM and I/D[1:0] settings as it writes data in the GRAM. The DFM bit sets the format to develop 16-bit data into the 18-bit data in 16-bit or 8-bit interface operation.

Note: When writing data in the GRAM via system interface while using the RGB interface, make sure that write operations via two interfaces that do not conflict one another.

Table 58 GRAM data and corresponding LCD grayscale level (REV =1)

GRAM data RGB	Grayscale level	
	Negative	Positive
6'h00	V31	V0
6'h01	(V30+V31)/2	(V0+V1)/2
6'h02	V30	V1
6'h03	(V29+V30)/2	(V1+V2)/2
6'h04	V29	V2
6'h05	(V28+V29)/2	(V2+V3)/2
6'h06	V28	V3
6'h07	(V27+V28)/2	(V3+V4)/2
6'h08	V27	V4
6'h09	(V26+V27)/2	(V4+V5)/2
6'h0A	V26	V5
6'h0B	(V25+V26)/2	(V5+V6)/2
6'h0C	V25	V6
6'h0D	(V24+V25)/2	(V6+V7)/2
6'h0E	V24	V7
6'h0F	(V23+V24)/2	(V7+V8)/2
6'h10	V23	V8
6'h11	(V22+V23)/2	(V8+V9)/2
6'h12	V22	V9
6'h13	(V21+V22)/2	(V9+V10)/2
6'h14	V21	V10
6'h15	(V20+V21)/2	(V10+V11)/2
6'h16	V20	V11
6'h17	(V19+V20)/2	(V11+V12)/2
6'h18	V19	V12
6'h19	(V18+V19)/2	(V12+V13)/2
6'h1A	V18	V13
6'h1B	(V17+V18)/2	(V13+V14)/2
6'h1C	V17	V14
6'h1D	(V16+V17)/2	(V14+V15)/2
6'h1E	V16	V15
6'h1F	(V15+V16)/2	(V15+V16)/2

GRAM data RGB	Grayscale level	
	Negative	Positive
6'h20	V15	V16
6'h21	(V14+V15)/2	(V16+V17)/2
6'h22	V14	V17
6'h23	(V13+V14)/2	(V17+V18)/2
6'h24	V13	V18
6'h25	(12+V13)/2	(V18+V19)/2
6'h26	V12	V19
6'h27	(11V12)/2	(V19+V20)/2
6'h28	V11	V20
6'h29	(V10+V11)/2	(V20+V21)/2
6'h2A	V10	V21
6'h2B	(V9+V10)/2	(V21+V22)/2
6'h2C	V9	V22
6'h2D	(V8+V9)/2	(V22+V23)/2
6'h2E	V8	V23
6'h2F	(V7+V8)/2	(V23+V24)/2
6'h30	V7	V24
6'h31	(V6+V7)/2	(V24+V25)/2
6'h32	V6	V25
6'h33	(V5+V6)/2	(V25+V26)/2
6'h34	V5	V26
6'h35	(V4+V5)/2	(V26+V27)/2
6'h36	V4	V27
6'h37	(V3+V4)/2	(V27+V28)/2
6'h38	V3	V28
6'h39	(V2+V3)/2	(V28+V29)/2
6'h3A	V2	V29
6'h3B	(V1+V2)/2	(V29+V30)/2
6'h3C	V1	V30
6'h3D	(V0+V1)/2	(V30+V31)/2
6'h3E	(V1+2V0)/3	(V30+2V31)/3
6'h3F	V0	V31

Note: (Vn+Vn+1)/2, (V1+2V0)/3, (Vn+2Vn+1)/3 are the effective grayscale levels by FRC (frame rate control).

Table 59 GRAM data and corresponding LCD grayscale level (REV =0)

GRAM data RGB	Grayscale level	
	Negative	Positive
6'h00	V0	V31
6'h01	(V0+V1)/2	(V30+V31)/2
6'h02	V1	V30
6'h03	(V1+V2)/2	(V29+V30)/2
6'h04	V2	V29
6'h05	(V2+V3)/2	(V28+V29)/2
6'h06	V3	V28
6'h07	(V3+V4)/2	(V27+V28)/2
6'h08	V4	V27
6'h09	(V4+V5)/2	(V26+V27)/2
6'h0A	V5	V26
6'h0B	(V5+V6)/2	(V25+V26)/2
6'h0C	V6	V25
6'h0D	(V6+V7)/2	(V24+V25)/2
6'h0E	V7	V24
6'h0F	(V7+V8)/2	(V23+V24)/2
6'h10	V8	V23
6'h11	(V8+V9)/2	(V22+V23)/2
6'h12	V9	V22
6'h13	(V9+V10)/2	(V21+V22)/2
6'h14	V10	V21
6'h15	(V10+V11)/2	(V20+V21)/2
6'h16	V11	V20
6'h17	(V11+V12)/2	(V19+V20)/2
6'h18	V12	V19
6'h19	(V12+V13)/2	(V18+V19)/2
6'h1A	V13	V18
6'h1B	(V13+V14)/2	(V17+V18)/2
6'h1C	V14	V17
6'h1D	(V14+V15)/2	(V16+V17)/2
6'h1E	V15	V16
6'h1F	(V15+V16)/2	(V15+V16)/2

GRAM data RGB	Grayscale level	
	Negative	Positive
6'h20	V16	V15
6'h21	(V16+V17)/2	(V14+V15)/2
6'h22	V17	V14
6'h23	(V17+V18)/2	(V13+V14)/2
6'h24	V18	V13
6'h25	(V18+V19)/2	(12+V13)/2
6'h26	V19	V12
6'h27	(V19+V20)/2	(11V12)/2
6'h28	V20	V11
6'h29	(V20+V21)/2	(V10+V11)/2
6'h2A	V21	V10
6'h2B	(V21+V22)/2	(V9+V10)/2
6'h2C	V22	V9
6'h2D	(V22+V23)/2	(V8+V9)/2
6'h2E	V23	V8
6'h2F	(V23+V24)/2	(V7+V8)/2
6'h30	V24	V7
6'h31	(V24+V25)/2	(V6+V7)/2
6'h32	V25	V6
6'h33	(V25+V26)/2	(V5+V6)/2
6'h34	V26	V5
6'h35	(V26+V27)/2	(V4+V5)/2
6'h36	V27	V4
6'h37	(V27+V28)/2	(V3+V4)/2
6'h38	V28	V3
6'h39	(V28+V29)/2	(V2+V3)/2
6'h3A	V29	V2
6'h3B	(V29+V30)/2	(V1+V2)/2
6'h3C	V30	V1
6'h3D	(V30+V31)/2	(V0+V1)/2
6'h3E	(V30+2V31)/3	(V1+2V0)/3
6'h3F	V31	V0

Note: (Vn+Vn+1)/2, (V1+2V0)/3, (Vn+2Vn+1)/3 are the effective grayscale levels by FRC (frame rate control).

Read Data from GRAM (R202h)

R/W	RS	
R	1	RAM read data RD[17:0] is transferred via different data bus in different interface operation.

RD[17:0]: 18-bit data read from the GRAM. RAM read data RD[17:0] is transferred via different data bus in different interface operation.

When the R61509 reads data from the GRAM to the microcomputer, the first word read immediately after RAM address set is not outputted, so that it is invalid. Valid data is sent to the data bus when the R61509 reads out the second and subsequent word.

When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.

Note: This register is not available in RGB interface operation

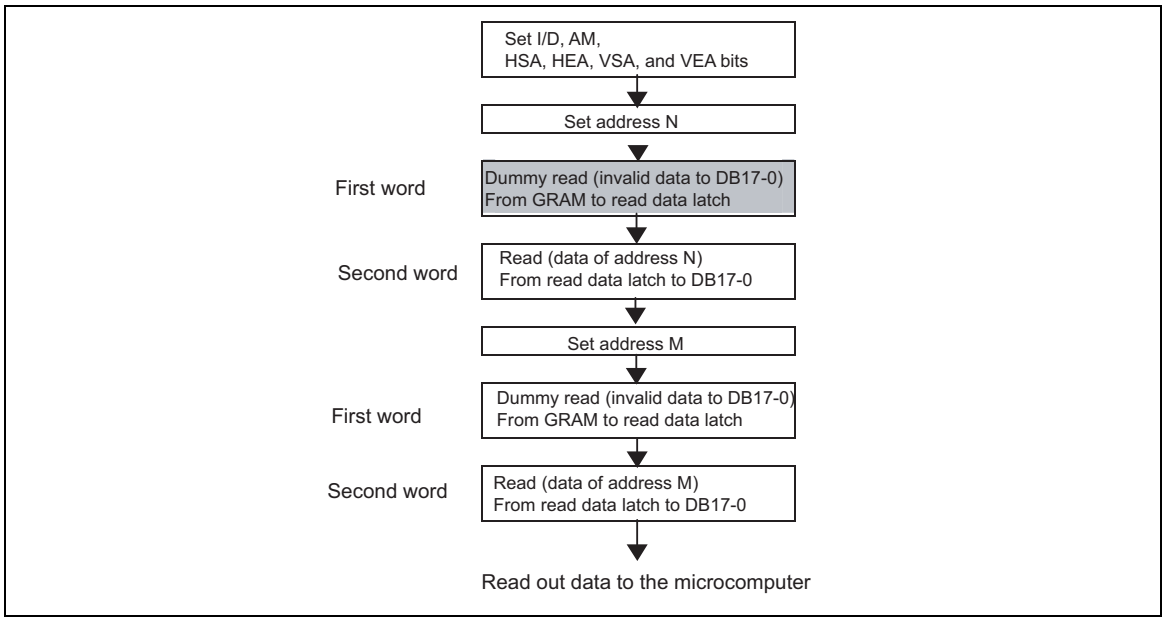


Figure 7 GRAM Read Sequence

Write/Read Data from/to NVM (R280h), VCOM High Voltage 1/2 (R281h/R282h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R280	R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	UID [3]	UID [2]	UID [1]	UID [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R281	R/W	1	0	0	0	0	0	0	0	0	0	0	0	VCM1 [4]	VCM1 [3]	VCM1 [2]	VCM1 [1]	VCM1 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R282	R/W	1	0	0	0	0	0	0	0	0	VCMSEL	0	0	VCM2 [4]	VCM2 [3]	VCM2 [2]	VCM2 [1]	VCM2 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

UID[3:0]: The data bits UID[3:0] are written to the designated address in NVM and the written data can be read out from NVM by instruction setting to this register. UID[3:0] can be used to write and read user identification code in NVM.

If UID value is rewritten, new setting is enabled.

VCM1[4:0]: Selects the factor of VREG1OUT to generate VCOMH. When enabling the setting valued in VCM1[4:0], make sure to set VCMSEL = 0.

When using the data written in NVM for setting the VCOMH level, the data bits VCM1[4:0] are written to the designated address in NVM and the written data can be read out from NVM by instruction setting to this register. When the data bits VCM2[4:0] are written in NVM before writing the data bits VCM1[4:0] to NVM, the VCM1[4:0] setting value written in NVM cannot be used for setting the VCOMH level.

Table 60

VCM1[4:0]	VCOMH voltage
5'h00	VREG1OUT x 0.69
5'h01	VREG1OUT x 0.70
5'h02	VREG1OUT x 0.71
5'h03	VREG1OUT x 0.72
5'h04	VREG1OUT x 0.73
5'h05	VREG1OUT x 0.74
5'h06	VREG1OUT x 0.75
5'h07	VREG1OUT x 0.76
5'h08	VREG1OUT x 0.77
5'h09	VREG1OUT x 0.78
5'h0A	VREG1OUT x 0.79
5'h0B	VREG1OUT x 0.80
5'h0C	VREG1OUT x 0.81
5'h0D	VREG1OUT x 0.82
5'h0E	VREG1OUT x 0.83
5'h0F	VREG1OUT x 0.84

VCM1[4:0]	VCOMH voltage
5'h10	VREG1OUT x 0.85
5'h11	VREG1OUT x 0.86
5'h12	VREG1OUT x 0.87
5'h13	VREG1OUT x 0.88
5'h14	VREG1OUT x 0.89
5'h15	VREG1OUT x 0.90
5'h16	VREG1OUT x 0.91
5'h17	VREG1OUT x 0.92
5'h18	VREG1OUT x 0.93
5'h19	VREG1OUT x 0.94
5'h1A	VREG1OUT x 0.95
5'h1B	VREG1OUT x 0.96
5'h1C	VREG1OUT x 0.97
5'h1D	VREG1OUT x 0.98
5'h1E	VREG1OUT x 0.99
5'h1F	VREG1OUT x 1.00

Notes: 1. Make sure the VCOMH level is set between 3.0V to (DDVDH-0.5)V.
2. The above setting is enabled when selecting internal electronic volume for setting the VCOMH level.

VCM2[4:0]: Selects the factor of VREG1OUT to generate VCOMH. When enabling the setting valued in VCM2[4:0], make sure to set VCMSEL = 1. The function of VCM2[4:0] instruction is the same as that of VCM1[4:0].

Write the setting value in VCM2[4:0] bits and VCMSEL = 1 in the designated addresses of NVM, when reading out the setting value written in NVM for VCOMH level setting and the data is already written in the designated address of VCM1[4:0] in the NVM. The VCM2[4:0] data bits written in NVM can be read out via VCM2[4:0] setting for setting the VCOMH level.

Table 61

VCM2[4:0]	VCOMH voltage	VCM2[4:0]	VCOMH voltage
5'h00	VREG1OUT x 0.69	5'h10	VREG1OUT x 0.85
5'h01	VREG1OUT x 0.70	5'h11	VREG1OUT x 0.86
5'h02	VREG1OUT x 0.71	5'h12	VREG1OUT x 0.87
5'h03	VREG1OUT x 0.72	5'h13	VREG1OUT x 0.88
5'h04	VREG1OUT x 0.73	5'h14	VREG1OUT x 0.89
5'h05	VREG1OUT x 0.74	5'h15	VREG1OUT x 0.90
5'h06	VREG1OUT x 0.75	5'h16	VREG1OUT x 0.91
5'h07	VREG1OUT x 0.76	5'h17	VREG1OUT x 0.92
5'h08	VREG1OUT x 0.77	5'h18	VREG1OUT x 0.93
5'h09	VREG1OUT x 0.78	5'h19	VREG1OUT x 0.94
5'h0A	VREG1OUT x 0.79	5'h1A	VREG1OUT x 0.95
5'h0B	VREG1OUT x 0.80	5'h1B	VREG1OUT x 0.96
5'h0C	VREG1OUT x 0.81	5'h1C	VREG1OUT x 0.97
5'h0D	VREG1OUT x 0.82	5'h1D	VREG1OUT x 0.98
5'h0E	VREG1OUT x 0.83	5'h1E	VREG1OUT x 0.99
5'h0F	VREG1OUT x 0.84	5'h1F	VREG1OUT x 1.00

Notes: 1. Make sure the VCOMH level is set between 3.0V to (DDVDH-0.5)V.

16 The above setting is enabled when selecting internal electronic volume for setting the VCOMH level.

VCMSEL: When VCMSEL = 0, VCM1[4:0] is selected. When VCMSEL = 1, VCM2[4:0] is selected.

Window Address Control

Window Horizontal RAM Address Start (R210h), Window Horizontal RAM Address End (R211h)

Window Vertical RAM Address Start (R212h), Window Vertical RAM Address End (R213h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R210	R/W	1	0	0	0	0	0	0	0	0	HSA [7]	HSA [6]	HSA [5]	HSA [4]	HSA [3]	HSA [2]	HSA [1]	HSA [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R211	R/W	1	0	0	0	0	0	0	0	0	HEA [7]	HEA [6]	HEA [5]	HEA [4]	HEA [3]	HEA [2]	HEA [1]	HEA [0]
	Default value		0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R212h	R/W	1	0	0	0	0	0	0	0	VSA [8]	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R213h	R/W	1	0	0	0	0	0	0	0	VEA [8]	VEA [7]	VEA [6]	VEA [5]	VEA [4]	VEA [3]	VEA [2]	VEA [1]	VEA [0]
	Default value		0	0	0	0	0	0	0	1	1	0	1	0	1	1	1	1

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HSA < HEA ≤ 8'hEF and 8'h04 ≤ HEA – HSA.

VSA[8:0], VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. See GRAM Address Map. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h1AF.

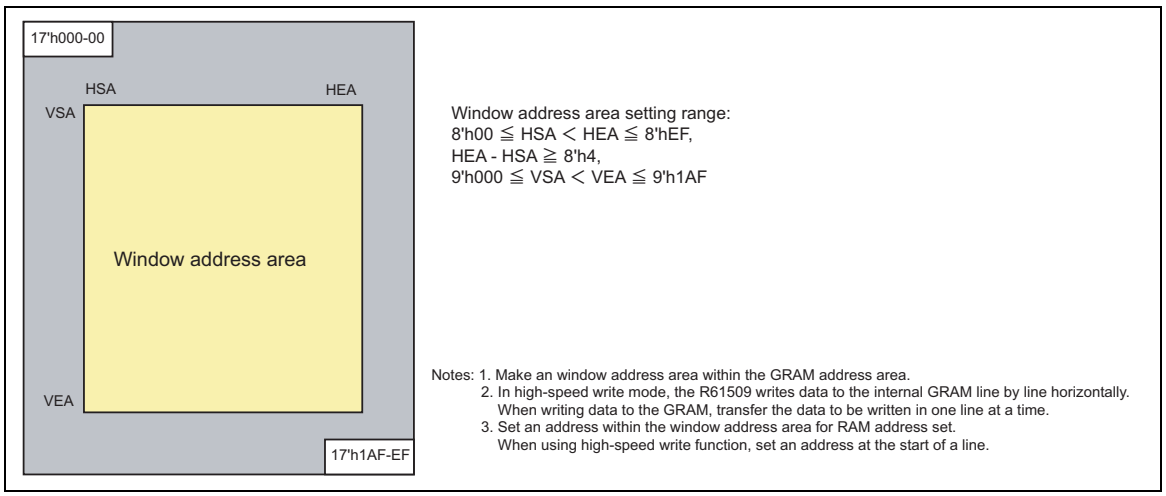


Figure 8 GRAM Address Map and Window Address Area

γ Control

γ Control 1 ~ 14 (R300h to R30Dh)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R300	R/W	1	0	0	0	0	0	P0KP1[2]	P0KP1[1]	P0KP1[0]	0	0	0	0	0	P0KP0[2]	P0KP0[1]	P0KP0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R301	R/W	1	0	0	0	0	0	P0KP3[2]	P0KP3[1]	P0KP3[0]	0	0	0	0	0	P0KP2[2]	P0KP2[1]	P0KP2[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R302	R/W	1	0	0	0	0	0	P0KP5[2]	P0KP5[1]	P0KP5[0]	0	0	0	0	0	P0KP4[2]	P0KP4[1]	P0KP4[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R303	R/W	1	0	0	0	0	0	0	P0FP1[1]	P0FP1[0]	0	0	0	0	0	0	P0FP0[1]	P0FP0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R304	R/W	1	0	0	0	0	0	0	P0FP3[1]	P0FP3[0]	0	0	0	0	0	0	P0FP2[1]	P0FP2[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R305	R/W	1	0	0	0	0	0	P0RP1[2]	P0RP1[1]	P0RP1[0]	0	0	0	0	0	P0RP0[2]	P0RP0[1]	P0RP0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R306	R/W	1	0	0	0	V0RP1[4]	V0RP1[3]	V0RP1[2]	V0RP1[1]	V0RP1[0]	0	0	0	V0RP0[4]	V0RP0[3]	V0RP0[2]	V0RP0[1]	V0RP0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R307	R/W	1	0	0	0	0	0	P0KN1[2]	P0KN1[1]	P0KN1[0]	0	0	0	0	0	P0KN0[2]	P0KN0[1]	P0KN0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R308	R/W	1	0	0	0	0	0	P0KN3[2]	P0KN3[1]	P0KN3[0]	0	0	0	0	0	P0KN2[2]	P0KN2[1]	P0KN2[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R309	R/W	1	0	0	0	0	0	P0KN5[2]	P0KN5[1]	P0KN5[0]	0	0	0	0	0	P0KN4[2]	P0KN4[1]	P0KN4[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R30A	R/W	1	0	0	0	0	0	0	P0FN1[1]	P0FN1[0]	0	0	0	0	0	0	P0FN0[1]	P0FN0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R30B	R/W	1	0	0	0	0	0	0	P0FN3[1]	P0FN3[0]	0	0	0	0	0	0	P0FN2[1]	P0FN2[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R30C	R/W	1	0	0	0	0	0	P0RN1[2]	P0RN1[1]	P0RN1[0]	0	0	0	0	0	P0RN0[2]	P0RN0[1]	P0RN0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R30D	R/W	1	0	0	0	V0RN1[4]	V0RN1[3]	V0RN1[2]	V0RN1[1]	V0RN1[0]	0	0	0	V0RN0[4]	V0RN0[3]	V0RN0[2]	V0RN0[1]	V0RN0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

P0KP5-0[2:0]:	γ fine-adjustment register for positive polarity
P0FP3-0[1:0]:	γ fine-adjustment register for positive polarity
P0RP1-0[2:0]:	γ gradient-adjustment register for positive polarity
V0RP1-0[4:0]:	γ amplitude-adjustment register for positive polarity
P0KN5-0[2:0]:	γ fine-adjustment register for negative polarity
P0FN3-0[1:0]:	γ fine-adjustment register for negative polarity
P0RN1-0[2:0]:	γ gradient-adjustment register for negative polarity
V0RN1-0[4:0]:	γ amplitude-adjustment register for negative polarity

Base Image Display Control

Base Image Number of Line (R400h)

Base Image Display Control (R401h)

Base Image Vertical Scroll Control (R404h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R400	R/W	1	GS0	0	NL0 [5]	NL0 [4]	NL0 [3]	NL0 [2]	NL0 [1]	NL0 [0]	0	0	SCN0 [5]	SCN0 [4]	SCN0 [3]	SCN0 [2]	SCN0 [1]	SCN0 [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R401	R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL 0	VLE0	REV 0
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R404	R/W	1	0	0	0	0	0	0	0	VL0 [8]	VL0 [7]	VL0 [6]	VL0 [5]	VL0 [4]	VL0 [3]	VL0 [2]	VL0 [1]	VL0 [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GS0: Sets the direction of scan by the gate driver in the range determined by SCN0 and NL0 bits. The gate scan direction determined by setting GS0 = 0 is reversed by setting GS = 1. Set GS0 bit in combination with SM bits.

NL0[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL0[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

NDL0: Sets the source output level in non-lit display area. Settings are different to normally black panels and normally white panels.

Table 62

NDL0	Non-lit display area	
	Positive	Negative
0	V31	V0
1	V0	V31

Note: NDL0 setting is enabled in non-lit display area in partial display operation.

VLE0: Vertical scroll display enable bit. When VLE0 = 1, the R61509 starts displaying the base image from the line (of the physical display) determined by VL0[8:0] bits. VL0[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE0 = “0”.

Table 63

VLE	Base image
0	Fixed
1	Enable scrolling

REV0: Enables the grayscale inversion of the image by setting REV0 = 1. This enables the R61509 to display the same image from the same set of data whether the liquid crystal panel is normally black or white.

Table 64

REV 0	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V31	V0
	:	:	:
	18'h3FFFFF	V0	V31
1	18'h00000	V0	V31
	:	:	:
	18'h3FFFFF	V31	V0

Note: Source output of non-lit display area is set by NDL0 bit during partial display mode.

VL0[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL0.

Table 65

NL0[5:0]	Number of Lines	NL0[5:0]	Number of Lines	NL0[5:0]	Number of Lines
6'h00	Setting inhibited	6'h13	160	6'h26	312
6'h01	16 (lines)	6'h14	168	6'h27	320
6'h02	24	6'h15	176	6'h28	328
6'h03	32	6'h16	184	6'h29	336
6'h04	40	6'h17	192	6'h2A	344
6'h05	48	6'h18	200	6'h2B	352
6'h06	56	6'h19	208	6'h2C	360
6'h07	64	6'h1A	216	6'h2D	368
6'h08	72	6'h1B	224	6'h2E	376
6'h09	80	6'h1C	232	6'h2F	384
6'h0A	88	6'h1D	240	6'h30	392
6'h0B	96	6'h1E	248	6'h31	400
6'h0C	104	6'h1F	256	6'h32	408
6'h0D	112	6'h20	264	6'h33	416
6'h0E	120	6'h21	272	6'h34	424
6'h0F	128	6'h22	280	6'h35	432
6'h10	136	6'h23	288	6'h36-6'h3F	Setting inhibited
6'h11	144	6'h24	296		
6'h12	152	6'h25	304		

Table 66

SCN0[5:0]	Gate Line No (Scan start position)			
	SM=0		SM=1	
	GS0=0	GS0=1	GS0=0	GS0=1
6'h00	G1	G432	G1	G432
6'h01	G9	G424	G17	G416
6'h02	G17	G416	G33	G400
6'h03	G25	G408	G49	G384
6'h04	G33	G400	G65	G368
6'h05	G41	G392	G81	G352
6'h06	G49	G384	G97	G336
6'h07	G57	G376	G113	G320
6'h08	G65	G368	G129	G304
6'h09	G73	G360	G145	G288
6'h0A	G81	G352	G161	G272
6'h0B	G89	G344	G177	G256
6'h0C	G97	G336	G193	G240
6'h0D	G105	G328	G209	G224
6'h0E	G113	G320	G225	G208
6'h0F	G121	G312	G241	G192
6'h10	G129	G304	G257	G176
6'h11	G137	G296	G273	G160
6'h12	G145	G288	G289	G144
6'h13	G153	G280	G305	G128
6'h14	G161	G272	G321	G112
6'h15	G169	G264	G337	G96
6'h16	G177	G256	G353	G80
6'h17	G185	G248	G369	G64
6'h18	G193	G240	G385	G48
6'h19	G201	G232	G401	G32
6'h1A	G209	G224	G417	G16
6'h1B	G217	G216	G2	G431
6'h1C	G225	G208	G18	G415
6'h1D	G233	G200	G34	G399
6'h1E	G241	G192	G50	G383
6'h1F	G249	G184	G66	G367
6'h20	G257	G176	G82	G351
6'h21	G265	G168	G98	G335
6'h22	G273	G160	G114	G319
6'h23	G281	G152	G130	G303
6'h24	G289	G144	G146	G287
6'h25	G297	G136	G162	G271
6'h26	G305	G128	G178	G255
6'h27	G313	G120	G194	G239
6'h28	G321	G112	G210	G223
6'h29	G329	G104	G226	G207
6'h2A	G337	G96	G242	G191
6'h2B	G345	G88	G258	G175
6'h2C	G353	G80	G274	G159
6'h2D	G361	G72	G290	G143
6'h2E	G369	G64	G306	G127
6'h2F	G377	G56	G322	G111
6'h30	G385	G48	G338	G95
6'h31	G393	G40	G354	G79
6'h32	G401	G32	G370	G63
6'h33	G409	G24	G386	G47
6'h34	G417	G16	G402	G31
6'h35	G425	G8	G418	G15
6'h36-6'h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

Note: Make sure that gate scan end position (= gate scan start position + NL) does not exceed 432 lines.

Partial Display Control

Partial Image 1: Display Position (R500h), RAM Address (Start/End Line Address) (R501h/R502h)

Partial Image 2: Display Position (R503h), RAM Address (Start/End Line Address) (R504h/R505h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R 500h	R/W	1	0	0	0	0	0	0	0	PTDP 0[8]	PTDP 0[7]	PTDP 0[6]	PTDP 0[5]	PTDP 0[4]	PTDP 0[3]	PTDP 0[2]	PTDP 0[1]	PTDP 0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 501h	R/W	1	0	0	0	0	0	0	0	PTSA 0[8]	PTSA 0[7]	PTSA 0[6]	PTSA 0[5]	PTSA 0[4]	PTSA 0[3]	PTSA 0[2]	PTSA 0[1]	PTSA 0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 502h	R/W	1	0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 503h	R/W	1	0	0	0	0	0	0	0	PTDP 1[8]	PTDP 1[7]	PTDP 1[6]	PTDP 1[5]	PTDP 1[4]	PTDP 1[3]	PTDP 1[2]	PTDP 1[1]	PTDP 1[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 504h	R/W	1	0	0	0	0	0	0	0	PTSA 1[8]	PTSA 1[7]	PTSA 1[6]	PTSA 1[5]	PTSA 1[4]	PTSA 1[3]	PTSA 1[2]	PTSA 1[1]	PTSA 1[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 505h	R/W	1	0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[8:0]: Sets the display position of partial image 1.
PTDP1[8:0]: Sets the display position of partial image 2.
The display areas of the partial images 1 and 2 must not overlap each another. In setting, make sure that

Coordinates of partial image 1 display position: (PTDP0, PTDP0 + (PTEA0 – PTSA0))
Coordinates of partial image 2 display position: (PTDP1, PTDP1 + (PTEA1 – PTSA1))

Therefore,

Partial image 1 display area < Partial image 2 display area.

If PTDP0 = “9’h000”, the partial image 1 is displayed from the first line of the base image.

PTSA0[8:0] and PTEA0[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 1. In setting, make sure that PTSA0 ≤ PTEA0.

PTSA1[8:0] and PTEA1[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 2. In setting, make sure that PTSA1 ≤ PTEA1.

Pin Control

Software Reset (R600h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRST
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRST: When SRST = 1, software is reset.
When SRST = 0, software reset is canceled.

When software reset is executed, instruction registers other than SRST, UID[3:0], VCM1[4:0], VCM2[4:0] and VCMSEL are initialized.

i80-i/F Endian Control (R606h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	0	0	0	0	0	TCREV[1]	0	0	0	0	0	0	0	TCREV[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TCREV[1:0]: Controls the endian setting (big/little endian: the order of receiving data) when transferring one-pixel data via i80 interface in multiple times. When setting a new value to TCREV[1:0], the order is changed from when the next instruction is executed.

Table 67

TCREV[1:0]	2 Transfers/Pixel	3 Transfers/Pixel
2'h0	Upper to lower ($1^{st} \rightarrow 2^{nd}$)	Upper to lower ($1^{st} \rightarrow 2^{nd} \rightarrow 3^{rd}$)
2'h1	Setting disabled	Setting disabled
2'h2	Setting disabled	Setting disabled
2'h2	Lower to upper ($2^{nd} \rightarrow 1^{st}$)	Lower to upper ($3^{rd} \rightarrow 2^{nd} \rightarrow 1^{st}$)

Notes: 1. In read operation, the data is transferred from upper bits to lower bits (big endian) regardless of TCREV[1:0] setting.
2. Make sure to set TCRV[1:0] when executing reset or exiting from shutdown mode.

NVM Control

NVM Access Control (R6F0h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R 6F0	R/W	1	0	0	0	0	0	0	0	0	TE	0	EOP [1]	EOP [0]	0	0	EAD [1]	EAD [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EAD [1:0]: Designates the address in NVM, where the data is written. Each address has particular data to be written.

Table 68

EAD[1:0]	Data written into NVM
2'h0	UID[3:0] (R280 IB3-0)
2'h1	VCM1 [4:0] (R281 IB4-0)
2'h2	VCMSEL, VCM2 [4:0] (R282 IB7, IB4-0)
2'h3	Setting disabled

EOP [1:0]: Writes into NVM or halts the write operation. Write-in data, on R280, R281 or R282 registers, is selected by EAD settings.

Table 69

EOP[1:0]	NVM control
2'h0	Halt
2'h1	Write
2'h2	Setting disabled
2'h3	Setting disabled

TE: Enable internal NVM control bit (EOP). Follow the NVM control sequence when setting TE.

●R61509 Instruction List

Rev0.0.5.5 2007.06.21

Major Category		Middle Category	Minor Category		Upper code								Lower code							
Index上位			Index	Commands	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
–	Index		—	Index	0	0	0	0	0	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID21	ID0
0**	Display control	00*	000h	Device code read	0	0	0	1	0	1	0	1	0	0	0	0	1	0	0	1
		Display control	001h	Driver output control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
			002h	LCD drive wave control	0	0	0	0	0	0	0	B/C[0] (0)	0	0	0	0	0	0	NW[1] (0)	NW[0] (0)
			003h	Entry mode	TRI (0)	DFM[0] (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	ID[1] (1)	ID[0] (1)	AM (0)	0	EPF[1] (0)	EPF[0] (0)
			004-005h	Setting disabled																
			006h	Outline sharpening control	EGMODE (0)	0	0	0	0	0	AVST[2] (0)	AVST[1] (0)	AVST[0] (0)	ADST[2] (0)	ADST[1] (0)	ADST[0] (0)	DTHU[1] (0)	DTHU[0] (0)	DTHL[1] (0)	DTHL[0] (0)
			007h	Display control 1	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE0 (0)	0	VON (0)	GON (0)	DTE (0)	0	0	D[1] (0)	D[0] (0)
			008h	Display control 2	0	0	0	0	FP[3] (1)	FP[2] (0)	FP[1] (0)	FP[0] (0)	0	0	0	0	BP[3] (1)	BP[2] (0)	BP[1] (0)	BP[0] (0)
			009h	Display control 3	0	0	0	0	PTV (0)	PTS[2] (0)	PTS[1] (0)	PTS[0] (0)	0	0	PTG[1] (0)	PTG[0] (0)	ISC[3] (0)	ISC[2] (0)	ISC[1] (0)	ISC[0] (0)
			00Ah	Setting disabled																
			00Bh	Low power control 1	0	0	0	0	0	0	0	0	0	0	0	VEM[0] (0)	0	0	0	COL (0)
			00Ch	External display control 1	0	ENC[2] (0)	ENC[1] (0)	ENC[0] (0)	0	0	0	RM (0)	0	0	DM[1] (0)	DM[0] (0)	0	0	RIM[1] (0)	RIM[0] (0)
			00D-00Eh	Setting disabled																
			00Fh	External display control 2	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
		01*	010h	Panel interface control 1	0	0	0	0	0	0	DIVI[1] (0)	DIVI[0] (0)	0	0	0	RTNI[4] (1)	RTNI[3] (0)	RTNI[2] (1)	RTNI[1] (1)	RTNI[0] (1)
		Panel interface (Internal clock)	011h	Panel interface control 2	0	0	0	0	0	NOWI[2] (0)	NOWI[1] (0)	NOWI[0] (0)	0	0	0	0	0	SDTI[2] (0)	SDTI[1] (0)	SDTI[0] (0)
			012h	Panel interface control 3	0	0	0	0	0	0	VEQWI[1] (0)	VEQWI[0] (0)	0	0	0	0	0	SEQWI[2] (0)	SEQWI[1] (0)	SEQWI[0] (0)
			013-01Fh	Setting disabled																
		02*	020h	Panel interface control 4	0	0	0	0	0	0	DIVE[1] (1)	DIVE[0] (0)	0	RTNE[6] (0)	RTNE[5] (0)	RTNE[4] (1)	RTNE[3] (1)	RTNE[2] (1)	RTNE[1] (1)	RTNE[0] (0)
		Panel interface (External clock)	021h	Panel interface control 5	0	0	0	0	NOWE[3] (0)	NOWE[2] (0)	NOWE[1] (0)	NOWE[0] (0)	0	0	0	0	SDTE[3] (0)	SDTE[2] (0)	SDTE[1] (0)	SDTE[0] (0)
			022h	Panel interface control 6	0	0	0	0	0	VEQWE[2] (0)	VEQWE[1] (0)	VEQWE[0] (0)	0	0	0	0	SEQWE[3] (0)	SEQWE[2] (0)	SEQWE[1] (0)	SEQWE[0] (0)
			023-08Fh	Setting disabled																
		09*	090h	Frame marker control	FMKM (0)	FMI[2] (0)	FMI[1] (0)	FMI[0] (0)	0	0	0	FMP[8] (0)	FMP[7] (0)	FMP[6] (0)	FMP[5] (0)	FMP[4] (0)	FMP[3] (0)	FMP[2] (0)	FMP[1] (0)	FMP[0] (0)
			091h	Setting disabled																
			092h	MDDI sub-display control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SIM[1] (0)	SIM[0] (0)
		Frame marker	093-0FFh	Setting disabled																
1**	Power control		100h	Power control 1	0	SAP[1] (0)	SAP[0] (0)	SAP (0)	0	BT[2] (0)	BT[1] (0)	BT[0] (0)	APE (0)	AP[2] (0)	AP[1] (0)	AP[0] (0)	0	DSTB (0)	SLP (0)	0
			101h	Power control 2	0	0	0	0	0	DC1[2] (1)	DC1[1] (1)	DC1[0] (0)	0	DC0[2] (1)	DC0[1] (1)	DC0[0] (0)	0	VC[2] (0)	VC[1] (0)	VC[0] (0)
			102h	Power control 3	0	0	0	0	0	0	0	VCMR0[0] (0)	VREG1R (0)	0	PSON (0)	PON (0)	VRH[3] (0)	VRH[2] (0)	VRH[1] (0)	VRH[0] (0)
			103h	Power control 4	0	0	VCOMG (0)	VDV[4] (0)	VDV[3] (0)	VDV[2] (0)	VDV[1] (0)	VDV[0] (0)	0	0	0	0	0	0	0	0
			104-106h	Setting disabled																
			107h	Power control 5	0	0	0	0	0	0	0	0	0	0	0	DCM[0] (0)	DCT[3] (0)	DCT[2] (0)	DCT[1] (0)	DCT[0] (0)
			108-10Fh	Setting disabled																
			110h	Power control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE (0)
			111h	Setting disabled																
			112h	Power control 7	0	0	0	0	0	0	TBT[1] (1)	TBT[0] (1)	0	1	1	0	0	0	0	0
			113-1FFh	Setting disabled																
2**	RAM access	20*	200h	RAM address set (Horizontal address)	0	0	0	0	0	0	0	0	AD[7] (0)	AD[6] (0)	AD[5] (0)	AD[4] (0)	AD[3] (0)	AD[2] (0)	AD[1] (0)	AD[0] (0)
		RAM read/write	201h	RAM address set (Vertical address)	0	0	0	0	0	0	0	AD[16] (0)	AD[15] (0)	AD[14] (0)	AD[13] (0)	AD[12] (0)	AD[11] (0)	AD[10] (0)	AD[9] (0)	AD[8] (0)
			202h	Write data to /Read data from GRAM	Allocations of RAM write data RD[17:0]/RD[17:0] are different according to interface format.															
			203-20Fh	Setting disabled																
		21*	210h	Window horizontal RAM address start	0	0	0	0	0	0	0	0	HSA[7] (0)	HSA[6] (0)	HSA[5] (0)	HSA[4] (0)	HSA[3] (0)	HSA[2] (0)	HSA[1] (0)	HSA[0] (0)
		Window address	211h	Window horizontal RAM address end	0	0	0	0	0	0	0	0	HEA[7] (1)	HEA[6] (1)	HEA[5] (1)	HEA[4] (0)	HEA[3] (1)	HEA[2] (1)	HEA[1] (1)	HEA[0] (1)
			212h	Window vertical RAM address start	0	0	0	0	0	0	0	VSA[8] (0)	VSA[7] (0)	VSA[6] (0)	VSA[5] (0)	VSA[4] (0)	VSA[3] (0)	VSA[2] (0)	VSA[1] (0)	VSA[0] (0)
			213h	Window vertical RAM address end	0	0	0	0	0	0	0	VEA[8] (1)	VEA[7] (1)	VEA[6] (0)	VEA[5] (1)	VEA[4] (0)	VEA[3] (1)	VEA[2] (1)	VEA[1] (1)	VEA[0] (1)
			214-27Fh	Setting disabled																
		28*	280h	Write/Read Data from/to NVM	0	0	0	0	0	0	0	0	0	0	0	0	UID[3] (0)	UID[2] (0)	UID[1] (0)	UID[0] (0)
		NVM read data	281h	Vcom High Voltage 1	0	0	0	0	0	0	0	0	0	0	0	VCM1[4] (0)	VCM1[3] (0)	VCM1[2] (0)	VCM1[1] (0)	VCM1[0] (0)
			282h	Vcom High Voltage 2	0	0	0	0	0	0	0	0	VCMSEL (0)	0	0	VCM2[4] (0)	VCM2[3] (0)	VCM2[2] (0)	VCM2[1] (0)	VCM2[0] (0)
			283-2FFh	Setting disabled																
3**	γ control	30*	300h	γ control 1	0	0	0	0	0	P0KP1[2] (0)	P0KP1[1] (0)	P0KP1[0] (0)	0	0	0	0	0	P0KP0[2] (0)	P0KP0[1] (0)	P0KP0[0] (0)
		γ control	301h	γ control 2	0	0	0	0	0	P0KP3[2] (0)	P0KP3[1] (0)	P0KP3[0] (0)	0	0	0	0	0	P0KP2[2] (0)	P0KP2[1] (0)	P0KP2[0] (0)
			302h	γ control 3	0	0	0	0	0	P0KP5[2] (0)	P0KP5[1] (0)	P0KP5[0] (0)	0	0	0	0	0	P0KP4[2] (0)	P0KP4[1] (0)	P0KP4[0] (0)
			303h	γ control 4	0	0	0	0	0	0	P0FP1[1] (0)	P0FP1[0] (0)	0	0	0	0	0	0	P0FP0[1] (0)	P0FP0[0] (0)
			304h	γ control 5	0	0	0	0	0	0	P0FP3[1] (0)	P0FP3[0] (0)	0	0	0	0	0	0	P0FP2[1] (0)	P0FP2[0] (0)
			305h	γ control 6	0	0	0	0	0	P0RP1[2] (0)	P0RP1[1] (0)	P0RP1[0] (0)	0	0	0	0	0	P0RP0[2] (0)	P0RP0[1] (0)	P0RP0[0] (0)
			306h	γ control 7	0	0	0	V0RP1[4] (0)	V0RP1[3] (0)	V0RP1[2] (0)	V0RP1[1] (0)	V0RP1[0] (0)	0	0	0	V0RP0[4] (0)	V0RP0[3] (0)	V0RP0[2] (0)	V0RP0[1] (0)	V0RP0[0] (0)
			307h	γ control 8	0	0	0	0	0	P0KN1[2] (0)	P0KN1[1] (0)	P0KN1[0] (0)	0	0	0	0	0	P0KN0[2] (0)	P0KN0[1] (0)	P0KN0[0] (0)
			308h	γ control 9	0	0	0	0	0	P0KN3[2] (0)	P0KN3[1] (0)	P0KN3[0] (0)	0	0	0	0	0	P0KN2[2] (0)	P0KN2[1] (0)	P0KN2[0] (0)
			309h	γ control 10	0	0	0	0	0	P0KN5[2] (0)	P0KN5[1] (0)	P0KN5[0] (0)	0	0	0	0	0	P0KN4[2] (0)	P0KN4[1] (0)	P0KN4[0] (0)
			30Ah	γ control 11	0	0	0	0	0	0	P0FN1[1] (0)	P0FN1[0] (0)	0	0	0	0	0	0	P0FN0[1] (0)	P0FN0[0] (0)
			30Bh	γ control 12	0	0	0	0	0	0	P0FN3[1] (0)	P0FN3[0] (0)	0	0	0	0	0	0	P0FN2[1] (0)	P0FN2[0] (0)
			30Ch	γ control 13	0	0	0	0	0	P0RN1[2] (0)	P0RN1[1] (0)	P0RN1[0] (0)	0	0	0	0	0	P0RN0[2] (0)	P0RN0[1] (0)	P0RN0[0] (0)
			30Dh	γ control 14	0	0	0	V0RN1[4] (0)	V0RN1[3] (0)	V0RN1[2] (0)	V0RN1[1] (0)	V0RN1[0] (0)	0	0	0	V0RN0[4] (0)	V0RN0[3] (0)	V0RN0[2] (0)	V0RN0[1] (0)	V0RN0[0] (0)
			30E-3FFh	Setting disabled																
4**	Base image display		400h	Base image number of line	GS0 (0)	0	NL0[5] (0)	NL0[4] (0)	NL0[3] (0)	NL0[2] (0)	NL0[1] (0)	NL0[0] (0)	0	0	SCN0[5] (0)	SCN0[4] (0)	SCN0[3] (0)	SCN0[2] (0)	SCN0[1] (0)	SCN0[0] (0)
			401h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL0 (0)	VLE0 (0)	REV0 (0)
			402-403h	Setting disabled																
			404h	Base image vertical scroll control	0	0	0	0	0	0	0	VL0[8] (0)	VL0[7] (0)	VL0[6] (0)	VL0[5] (0)	VL0[4] (0)	VL0[3] (0)	VL0[2] (0)	VL0[1] (0)	VL0[0] (0)
			405-4FFh	Setting disabled																
5**	Partial display control		500h	Partial image 1: Display position	0	0	0	0	0	0	0	PTDP0[8] (0)	PTDP0[7] (0)	PTDP0[6] (0)	PTDP0[5] (0)	PTDP0[4] (0)	PTDP0[3] (0)	PTDP0[2] (0)	PTDP0[1] (0)	PTDP0[0] (0)
			501h	Partial image 1: RAM address start line address	0	0	0	0	0	0	0	PTSA0[8] (0)	PTSA0[7] (0)	PTSA0[6] (0)	PTSA0[5] (0)	PTSA0[4] (0)	PTSA0[3] (0)	PTSA0[2] (0)	PTSA0[1] (0)	PTSA0[0] (0)
			502h	Partial image 1: RAM address end line address	0	0	0	0	0	0	0	PTEA0[8] (0)	PTEA0[7] (0)	PTEA0[6] (0)	PTEA0[5] (0)	PTEA0[4] (0)	PTEA0[3] (0)	PTEA0[2] (0)	PTEA0[1] (0)	PTEA0[0] (0)
			503h	Partial image 2 display position	0	0	0	0	0	0	0	PTDP1[8] (0)	PTDP1[7] (0)	PTDP1[6] (0)	PTDP1[5] (0)	PTDP1[4] (0)	PTDP1[3] (0)	PTDP1[2] (0)	PTDP1[1] (0)	PTDP1[0] (0)
			504h	Partial image 2: RAM address start line address	0	0	0	0	0	0	0	PTSA1[8] (0)	PTSA1[7] (0)	PTSA1[6] (0)	PTSA1[5] (0)	PTSA1[4] (0)	PTSA1[3] (0)	PTSA1[2] (0)	PTSA1[1] (0)	PTSA1[0] (0)
			505h	Partial image 2: RAM address end line address	0	0	0	0	0	0	0	PTEA1[8] (0)	PTEA1[7] (0)	PTEA1[6] (0)	PTEA1[5] (0)	PTEA1[4] (0)	PTEA1[3] (0)	PTEA1[2] (0)	PTEA1[1] (0)	PTEA1[0] (0)
			506-5FFh	Setting disabled																
6**	Pin control	60*	600h	Software reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRST (0)
		Interface control	601-605h	Setting disabled																
			606h	I/F Endian Control	0	0	0	0	0	0	0	TCREV[1] (0)	0	0	0	0	0	0	0	TCREV[0] (0)
			607-6EFh	Setting disabled																
		6F*	6F0h	NVM access control	0	0	0	0	0	0	0	0	TE (0)	0	EOP[1] (0)	EOP[0] (0)	0	0	EAD[1] (0)	EAD[0] (0)
		NVM-I/F	6F1-FFFh	Setting disabled																

Note 1: Values in the parenthesis are default value.
Note 2: Do not access to instruction other than listed here.

Reset Function

The R61509 is initialized by the RESET input. During reset period, the R61509 is in a busy state and instruction from the microcomputer and GRAM access are not accepted. The R61509's internal power supply circuit unit is initialized also by the RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, GRAM access and initial instruction setting are prohibited.

1. Initial state of instruction bits (default)

See the instruction list. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization

The RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period (D1-0 = "00").

3. Output pin initial state * see Note

1.	LCD driver S1~S720	: GND
	G1~G432	: VGL (= GND)
2.	VCOM	: Halt (GND output)
3.	VCOMH	: VCI
4.	VCOML	: Halt (GND output)
5.	VREG1OUT	: VGS
6.	VCIOUT	: Hi-z
7.	VLOUT1	: VCI
8.	VLOUT2	: DDVDH (VCI clamp)
9.	VLOUT3	: GND
10.	VLOUT4	: GND
11.	FMARK	: Halt (GND output)
12.	Oscillator	: Oscillate
13.	SDO	: High level (IOVCC1) when IM2-0 = "10*"(serial interface)
		: Hi-z when IM2-0 ≠ "10*"(other than serial interface)

4. Initial state of input/output pins* see Note

1.	C11+	: Hi-z
2.	C11-	: Hi-z
3.	C12+	: Hi-z
4.	C12-	: Hi-z
5.	C13+	: VCI1 (= Hi-z)
6.	C13-	: GND
7.	C21+	: DDVDH (= VCI)
8.	C21-	: GND
9.	C22+	: DDVDH (= VCI)
10.	C22-	: GND
11.	C23+	: DDVDH (= VCI)
12.	C23-	: GND
13.	VDD	: VDD

Note: The above mentioned initial states of output and input pins are those of when the R61509's power supply circuit is connected as in Connection Example.

5 When a RESET input is entered into the R61509 while it is in shutdown mode, the R61509 starts up the inside logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable. For this reason, do not enter a RESET input in shutdown mode.

6 When transferring instruction in either two or three transfers via 8-/9-/16-bit interface, make sure to execute data transfer synchronization after reset operation.

Basic Mode Operation of the R61509

The basic operation modes of the R61509 are shown in the following diagram. When making a transition from one mode to another, refer to instruction setting sequence.

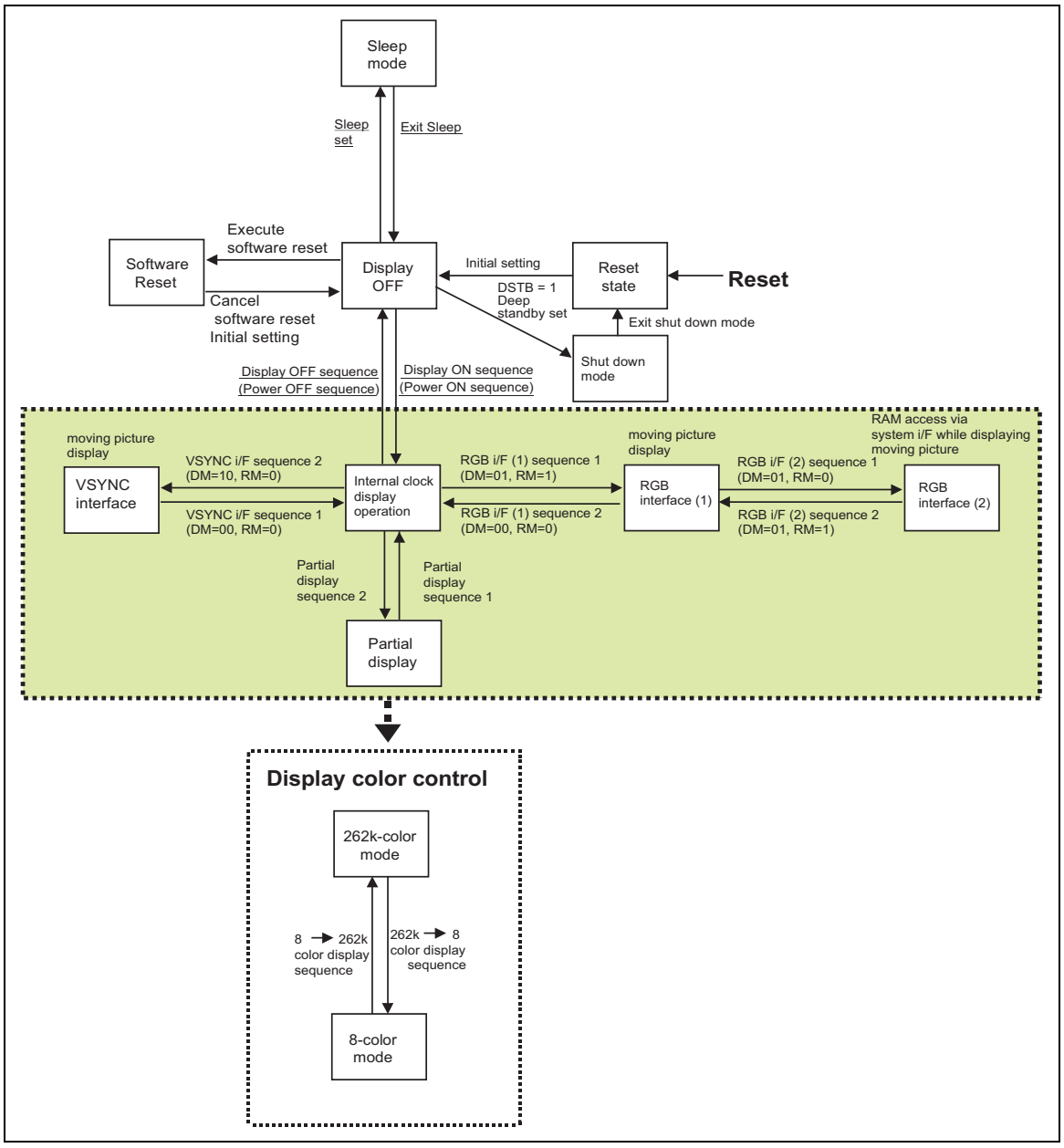


Figure 9

Interface and Data Format

The R61509 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The R61509 can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the R61509 supports RGB interface and VSYNC interface, which enables data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the R61509 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the R61509's GRAM so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the RAM area to write data for moving picture display, which enables displaying a moving picture and RAM data in other than the moving picture area simultaneously. To access the R61509's internal RAM in high speed with low power consumption, use high-speed write function (HWM = 1) in RGB or VSYNC interface operation.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The R61509 operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register (R0Ch). When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Table 70 Operation Modes

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes: 1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM1-0) while RGB interface is in operation.
4. See the "External Display Interface" section for the sequences when switching from one mode to another.
5. Use high-speed write function (HWM = 1) when writing data via RGB or VSYNC interface.

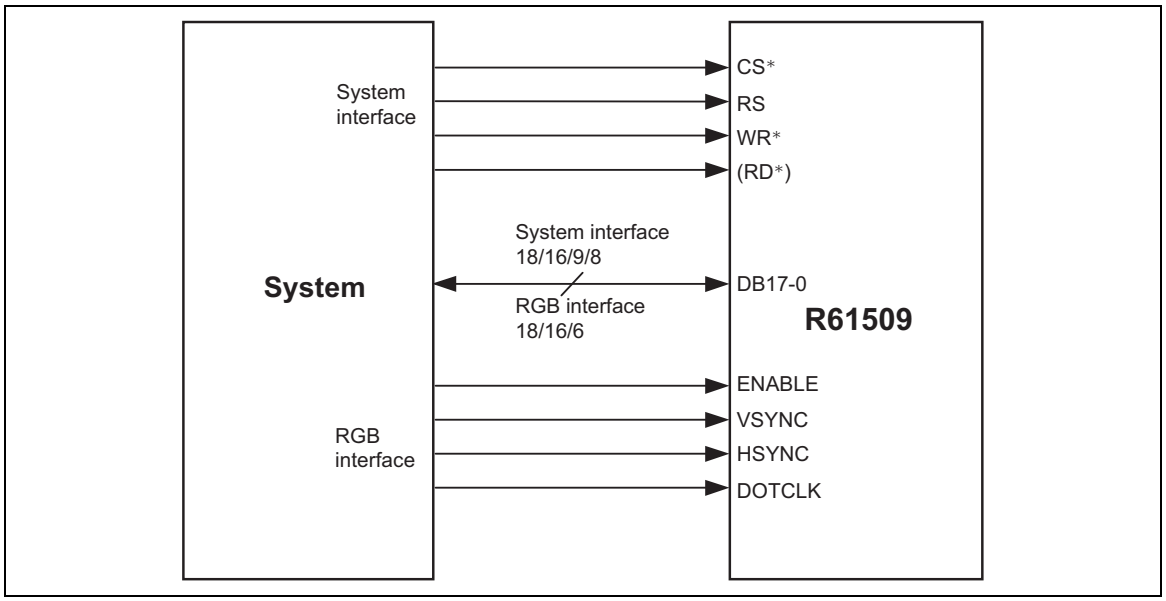


Figure 10

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

RGB interface operation (1)

The display operation is synchronized with frame synchronous signal (VSYNC), line synchronous signal (HSYNC), and dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied during the display operation via RGB interface.

The R61509 transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function can minimize the total number of data transfer for moving picture display by transferring only the data to be written in the moving picture RAM area when it is written and enables the R61509 to display a moving picture and the data in other than the moving picture RAM area simultaneously.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the R61509 by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with the setting of these periods.

RGB interface operation (2)

This mode enables the R61509 to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first. Then set an address in the RAM address set register and R22h in the index register.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the R61509 to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the "VSYNC Interface" section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the R61509 according to the instruction settings for these periods.

FMARK interface operation

In the FMARK interface operation, data is written to internal RAM via system interface synchronizing with the frame mark signal (FMARK), realizing tearing-less moving picture while using conventional system interface. In this case, there are restrictions in speed and method of writing RAM data. See "FMARK interface" for detail.

System Interface

The following are the kinds of system interfaces available with the R61509. The interface operation is selected by setting the IM2/1/0 pins. The system interface is used for instruction setting and RAM access. See also i80-i/F Endian Control (R606h) for the order of receiving data when data is transferred in multiple times.

Table 71 IM Bit Settings and System Interface

IM2	IM1	IM0	Interfacing Mode with MPU	DB Pins	Colors
0	0	0	80-system 18-bit interface	DB17-0	262,144
0	0	1	80-system 9-bit interface	DB17-9	262,144
0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144 *see Note1
0	1	1	80-system 8-bit interface	DB17-10	262,144 *see Note2
1	0	*	Clock synchronous serial interface	-	65,536
1	1	0	Setting inhibited	-	-
1	1	1	MDDI	MDDI_STB_P/M_B, MDDI_DATA_P/M_B	262,144 *see Note3

Notes: 1. 65,536 colors in 16-bit single transfer mode.
2. 262,144 colors is 8-bit 3-transfer mode. 65,536 colors in 8-bit 2-transfer mode.
3. 65,536 colors in MDDI operation (DFM = 1).

80-System 18-Bit Bus Interface

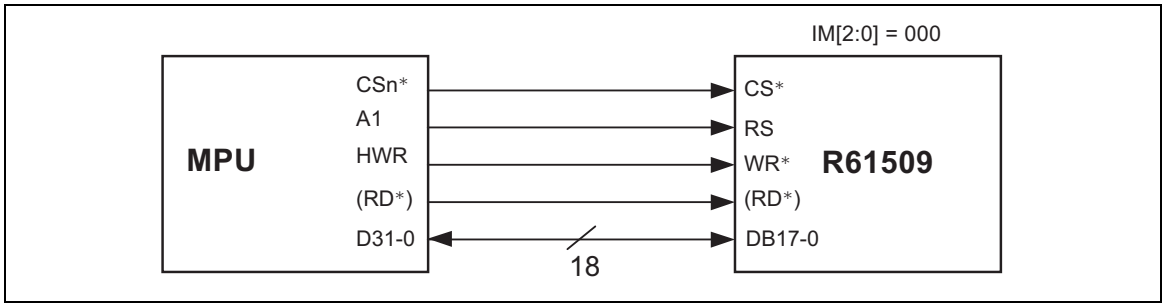


Figure 11 18-bit Interface

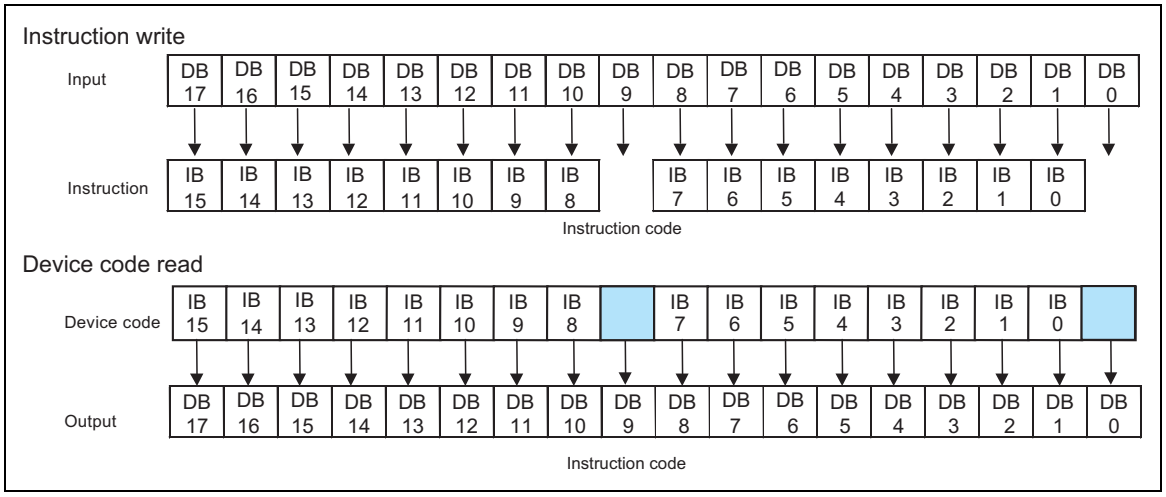


Figure 12 18-Bit Interface Data Format (Instruction Write / Device Code Read)

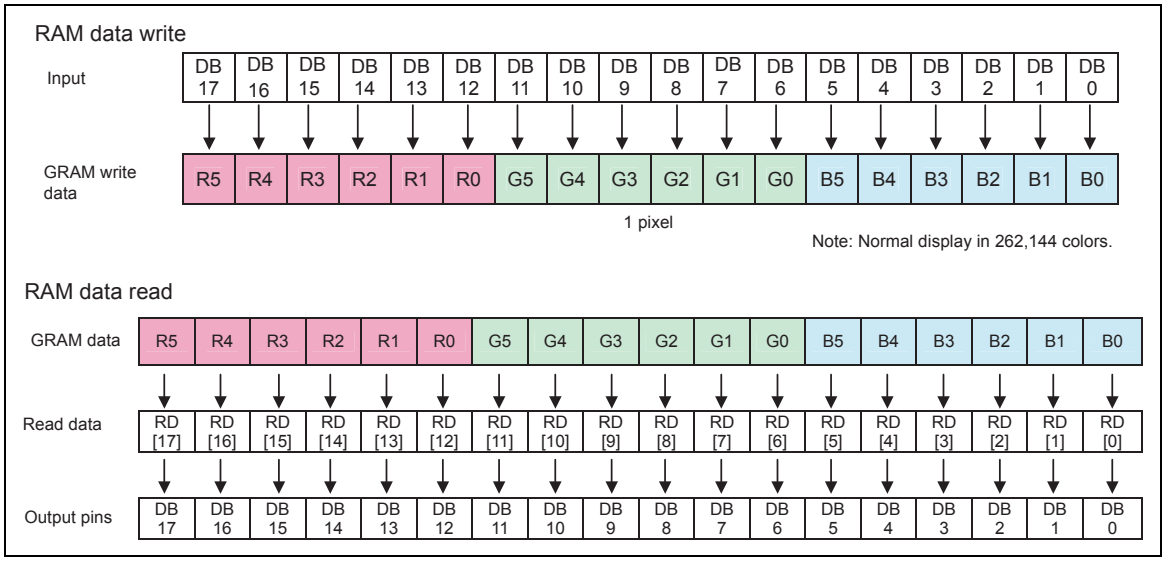


Figure 13 18-Bit Interface Data Format (RAM Data Write / RAM Data Read)

80-System 16-Bit Bus Interface

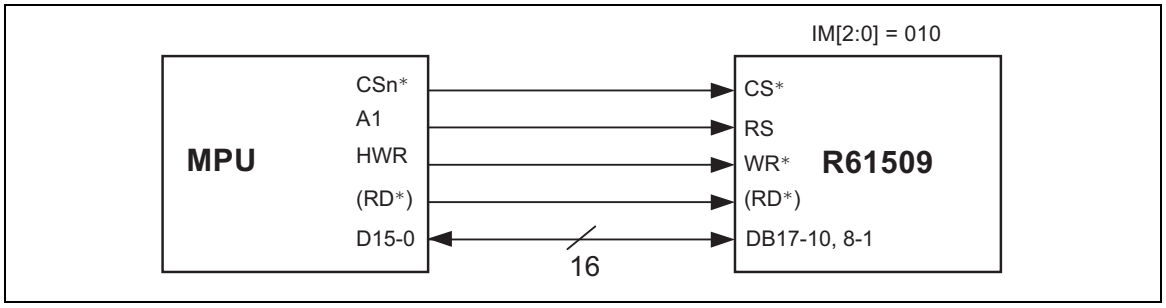


Figure 14 16-Bit Interface

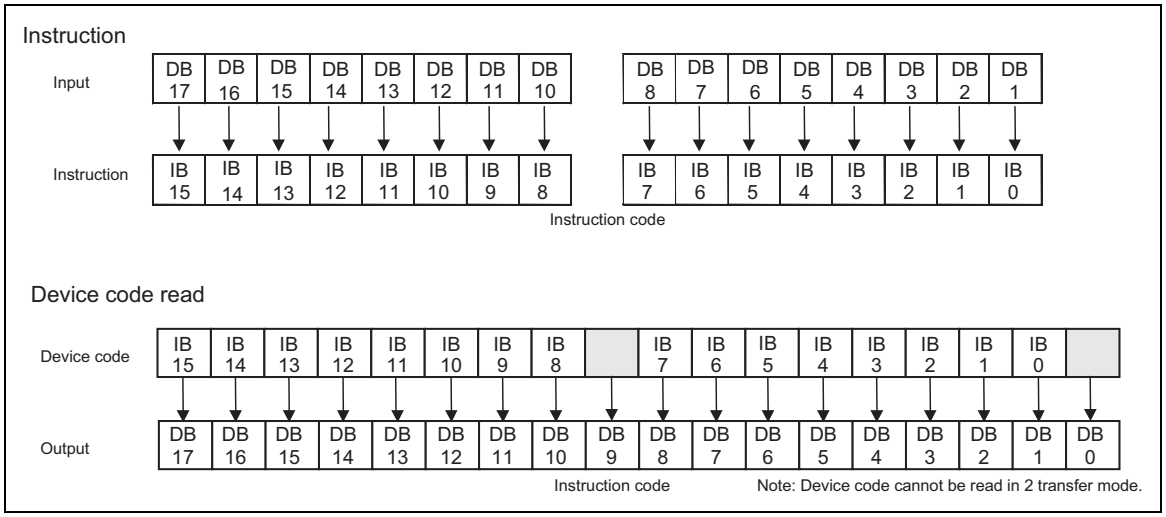


Figure 15 16-Bit Interface Data Format (Instruction Write / Device Code Read)

Figure 16 16-bit Interface Data Format (RAM Data Write)

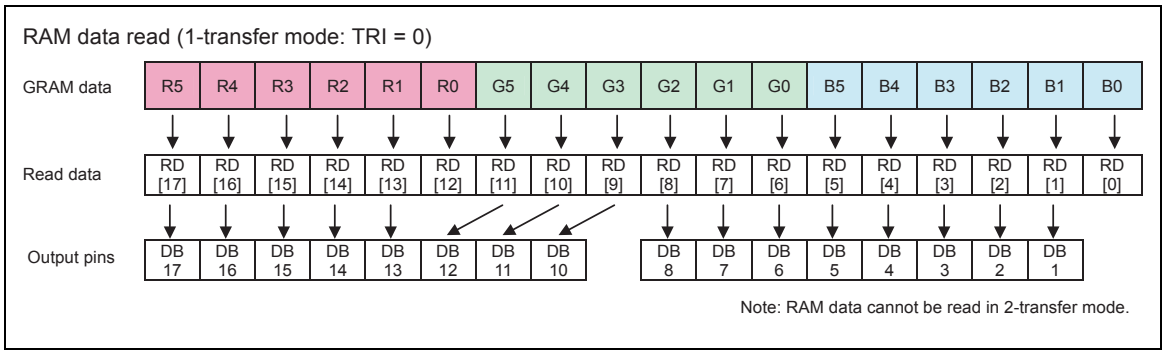


Figure 17 16-Bit Interface Data Format (RAM Data Read)

Data Transfer Synchronization in 16-Bit Bus Interface Operation

The R61509 supports data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 2/16 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

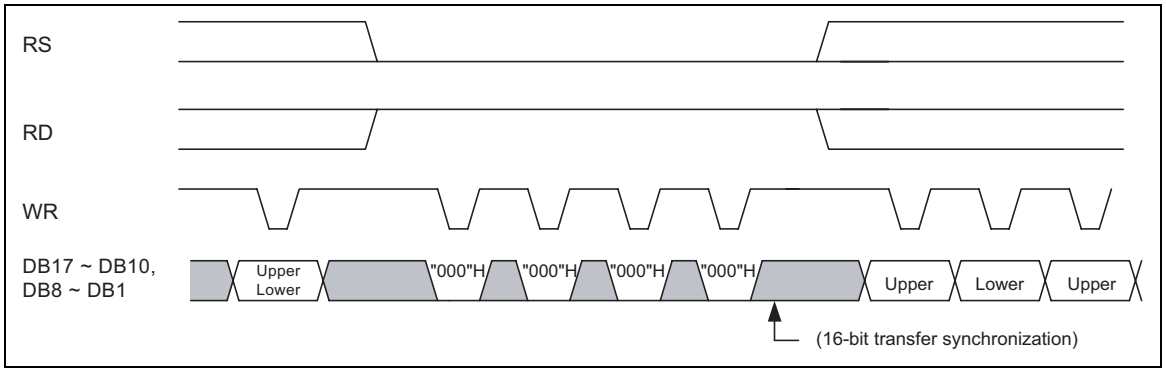


Figure 18 16-Bit Data Transfer Synchronization

80-System 9-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either IOVCC or IOGND level. When transferring the index register setting, make sure to write upper byte (8 bits).

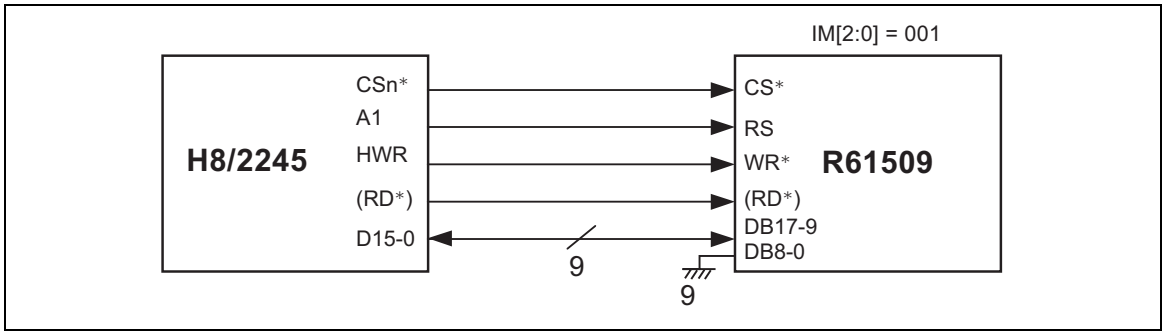


Figure 19 9-Bit Interface

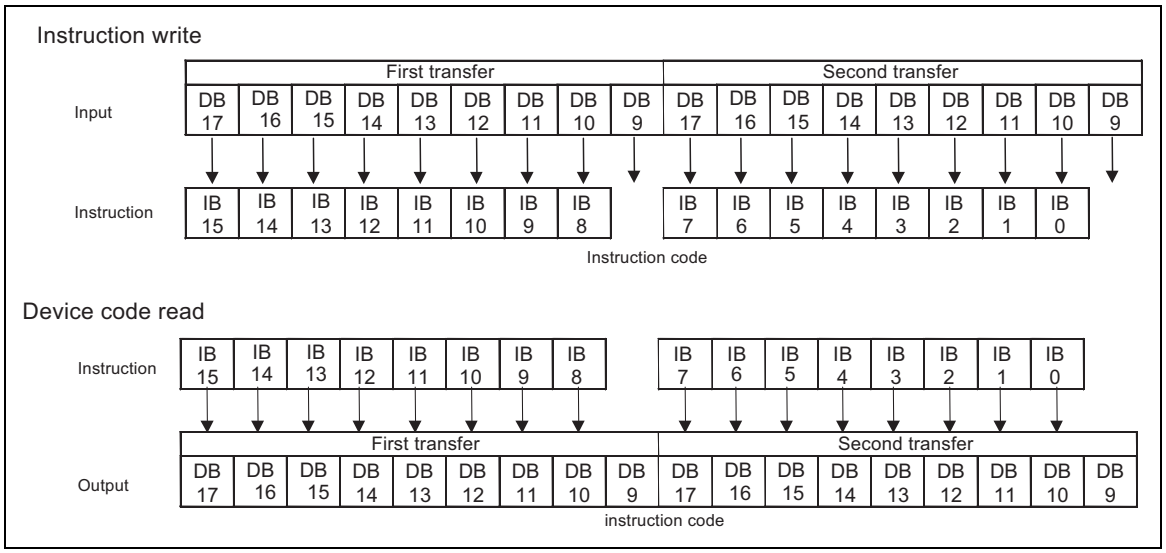


Figure 20 9-Bit Interface Data Format (Instruction Write / Device Code Read)

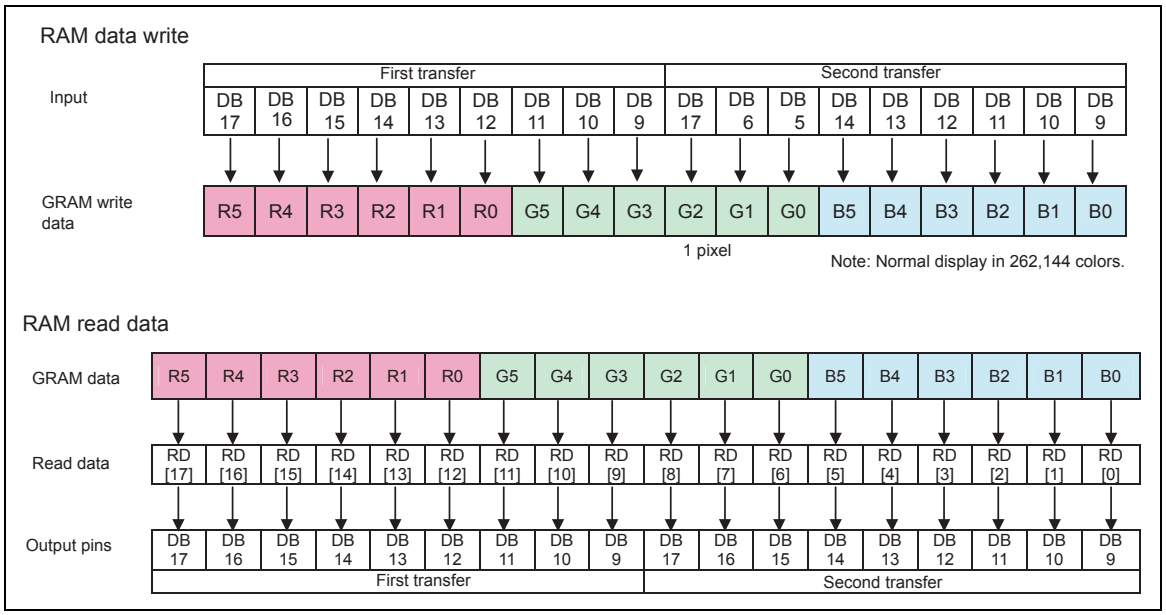


Figure 21 9-Bit Interface Data Format (RAM Data Write/ RAM Data Read)

Data Transfer Synchronization in 9-Bit Bus Interface Operation

The R61509 supports data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 9 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

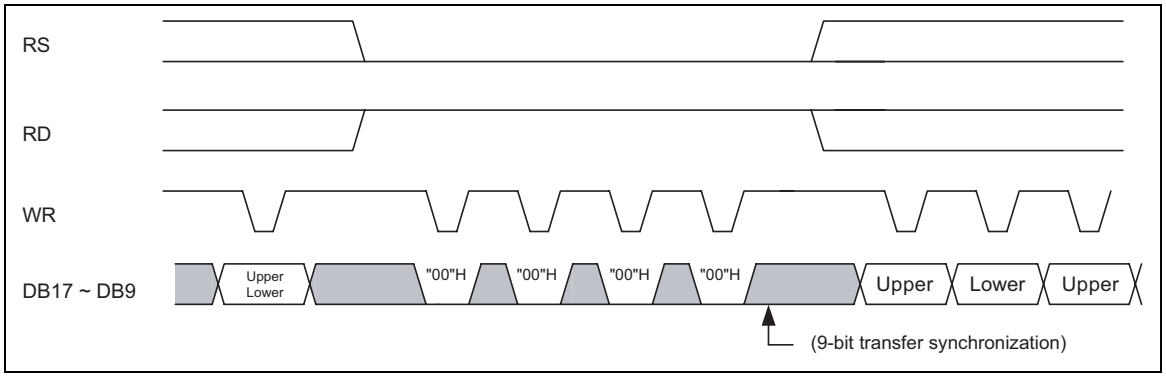


Figure 22 9-Bit Data Transfer Synchronization

80-System 8-Bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either IOVCC1 or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

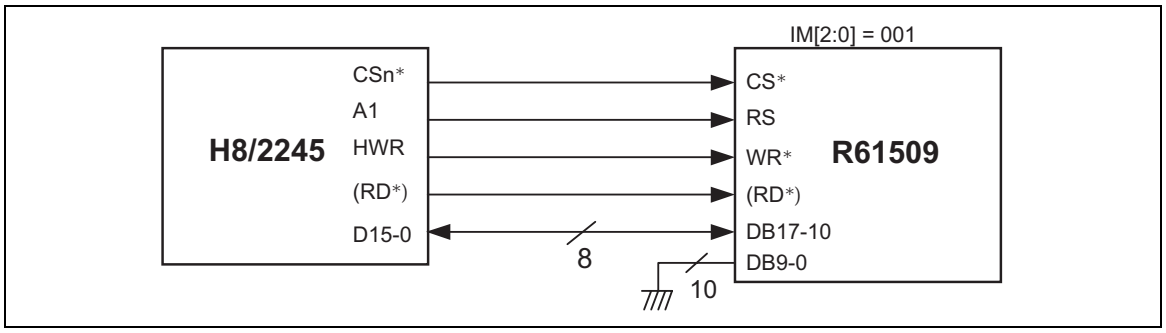


Figure 23 8-Bit Interface

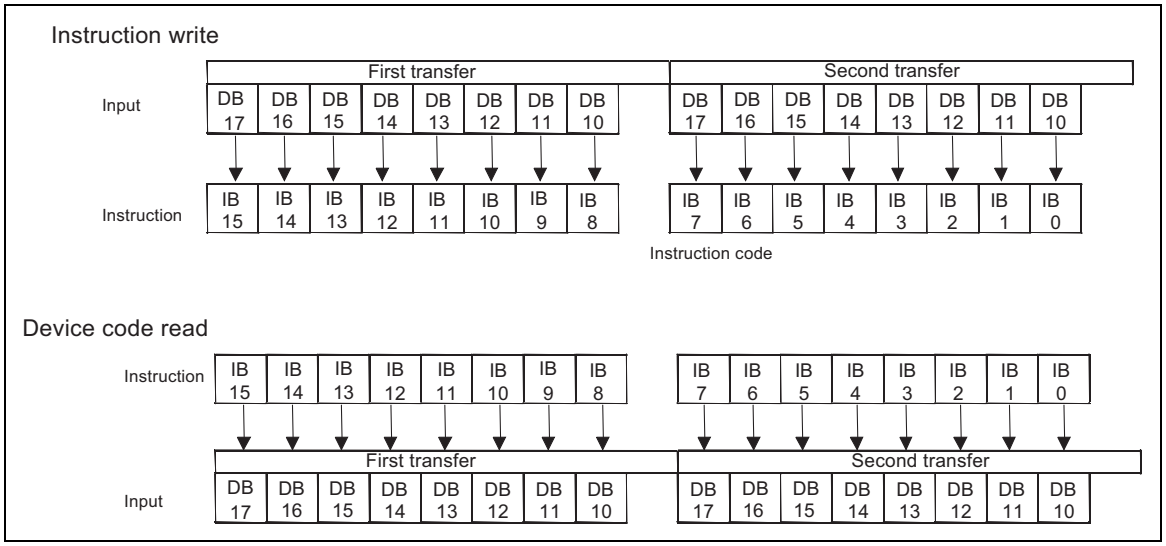


Figure 24 8-Bit Interface Data Format (Instruction Write / Device Code Read)

Note: RAM data cannot be read in the 3-transfer mode.

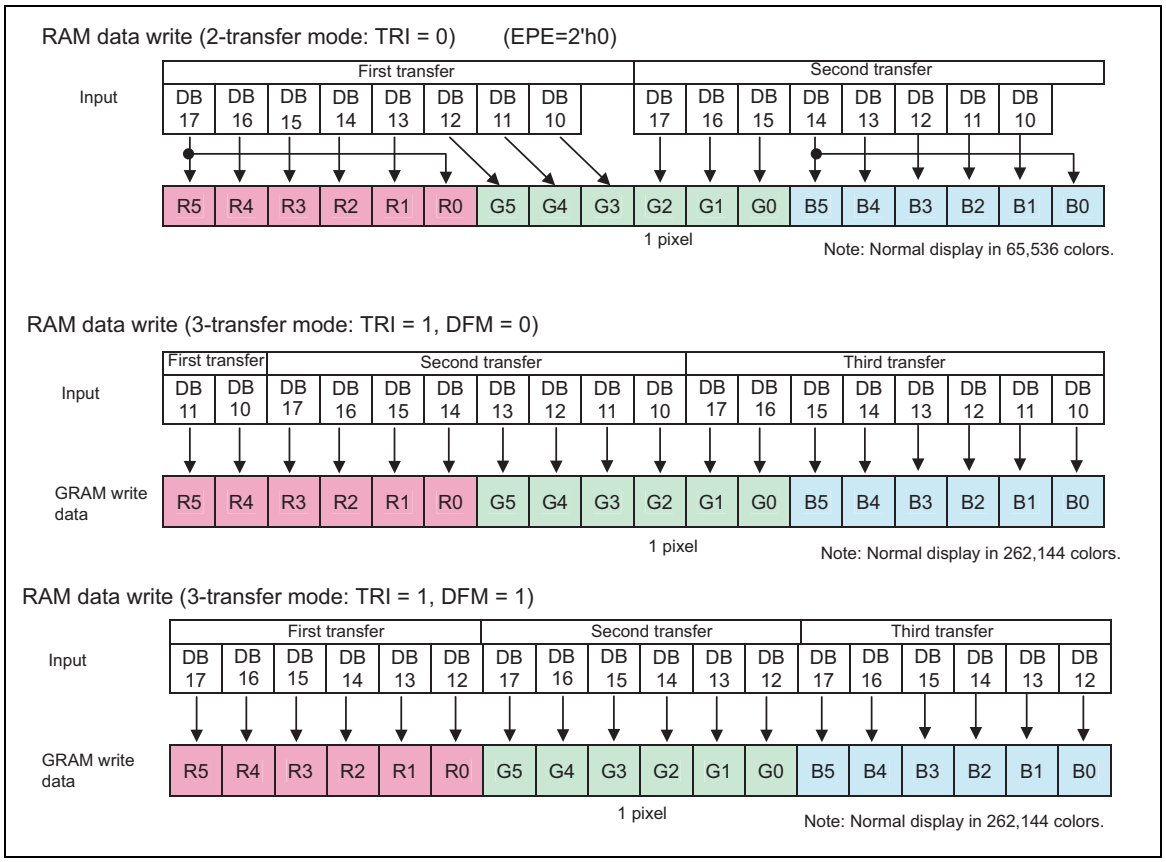


Figure 25 8-Bit Interface Data Format (RAM Data Write)

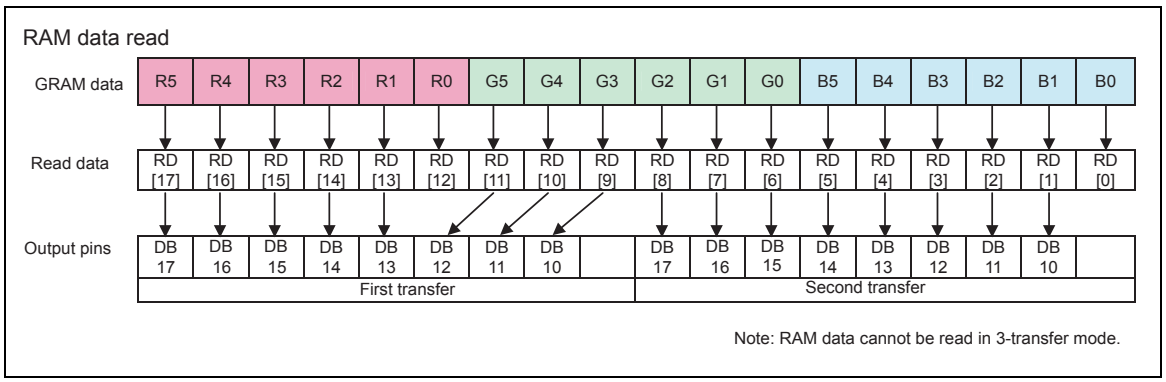


Figure 26 8-Bit Interface Data Format (RAM Data Read)

Data Transfer Synchronization in 8-bit Bus Interface operation

The R61509 supports data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 8 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

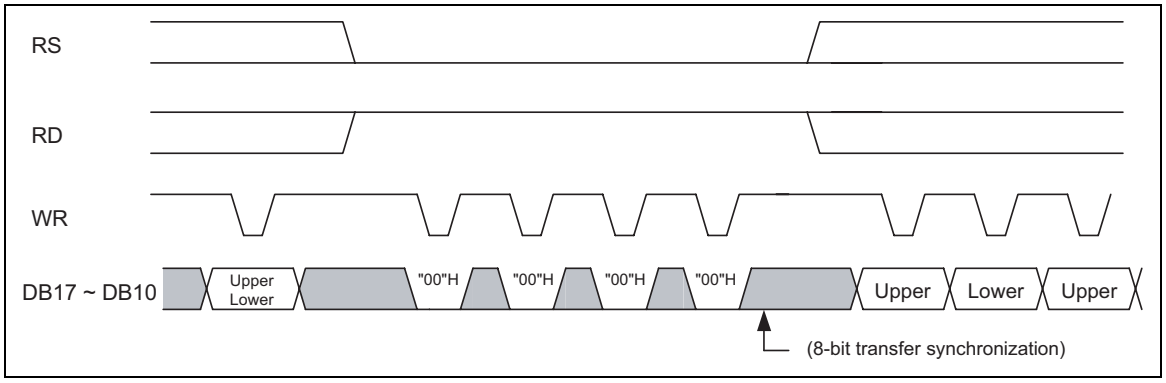


Figure 27 8-Bit Data Transfer Synchronization

Serial Interface

The serial interface is selected by setting the IM2/1 pins to the IOVCC1/IOGND1 levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVCC1 or GND level.

The R61509 recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The R61509 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the R61509 are compared and both 6-bit data match. Then, the R61509 starts taking in subsequent data. The least significant bit of the device identification code is determined by setting the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the R61509 because the seventh bit of the start byte is register select bit (RS). When RS = 0, index register write operation is executed. When RS = 1, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The R61509 receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The R61509 writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the R61509 starts transferring or receiving data in units of bytes. The R61509 transfers data from the MSB. The R61509's instruction consists of 16 bits and it is executed inside the R61509 after it is transferred in two bytes (16 bits: DB15-0) from the MSB. The R61509 expands RAM write data into 18 bits when writing them to the internal GRAM. The first byte received by the R61509 following the start byte is recognized as the upper eight bits of instruction and the second byte is recognized as the lower 8 bits of instruction.

When reading data from the GRAM, valid data is not transferred to the data bus until first five bytes of data are read from the GRAM following the start byte. The R61509 sends valid data to the data bus when it reads the sixth and subsequent byte data.

Table 72 Start Byte Format

Transferred Bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: The ID bit is determined by setting the IM0/ID pin.

Table 73 Functions of RS, R/W Bits

RS	R/W	Function
0	0	Set index register
0	1	Setting inhibited
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

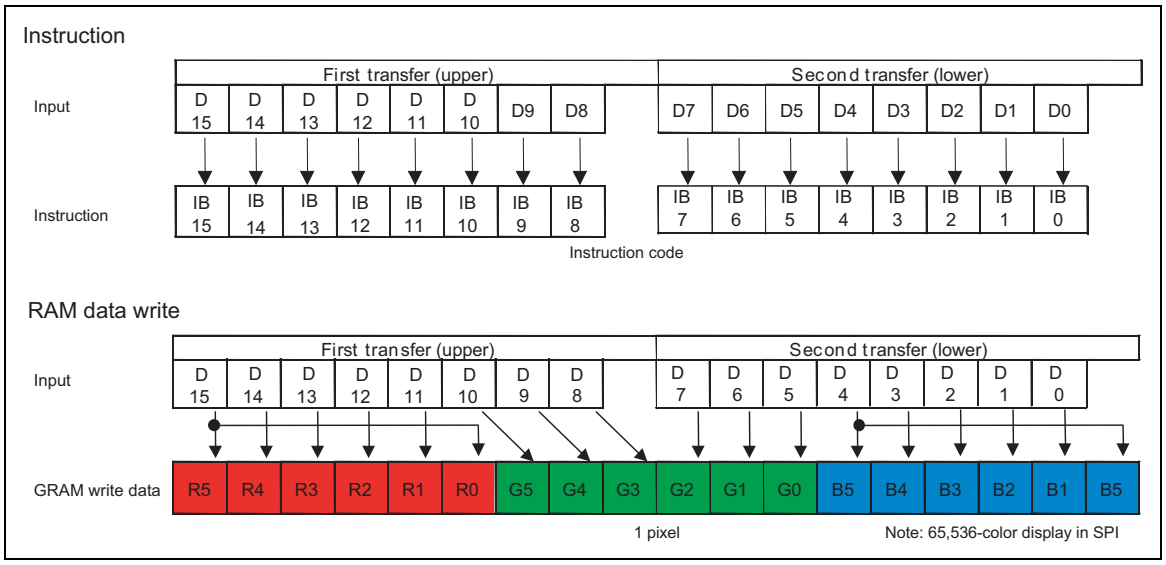


Figure 28 Serial Interface Data Format

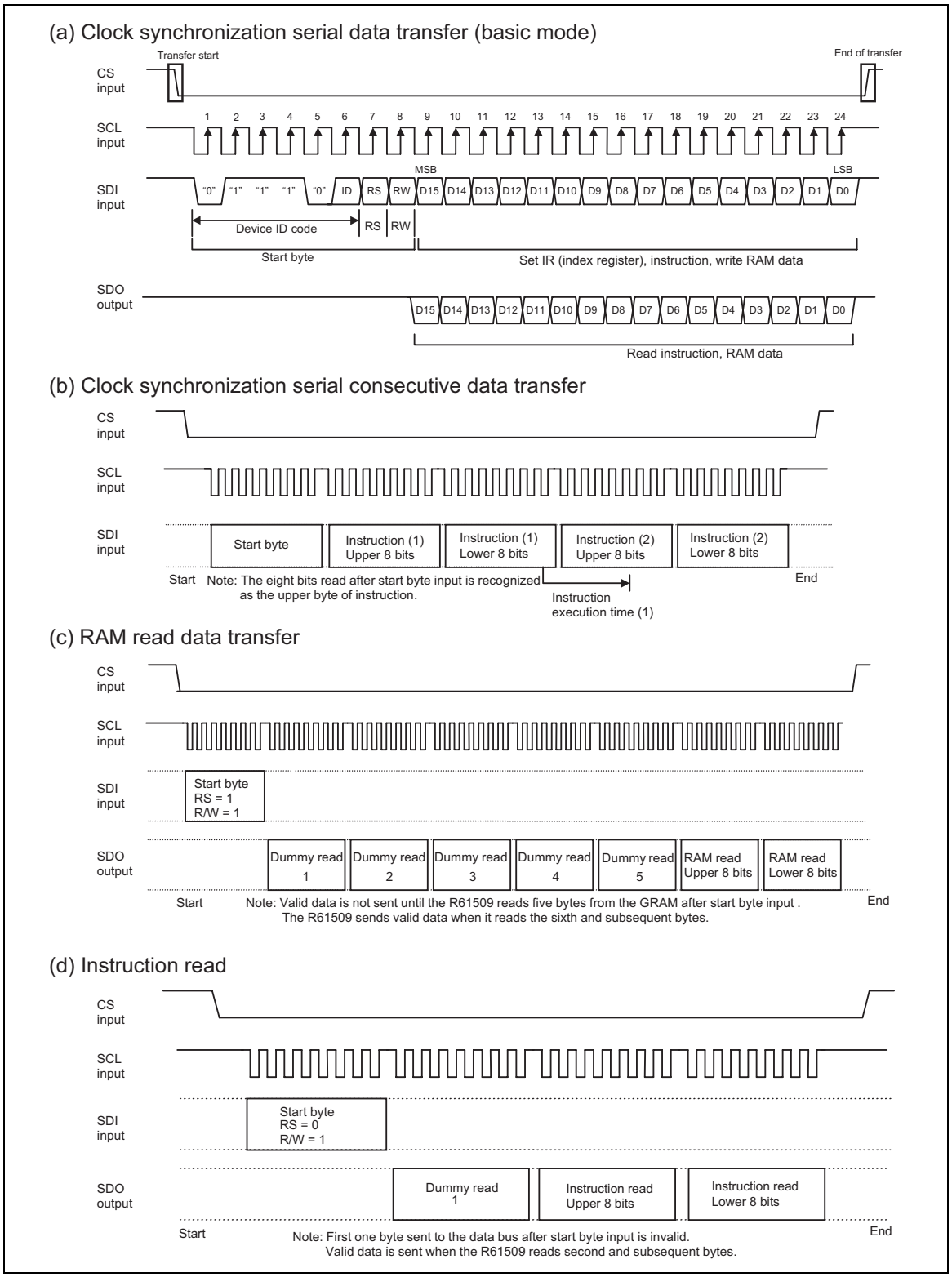


Figure 29 Data Transfer in Serial Interface

VSYNC Interface

The R61509 supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation.

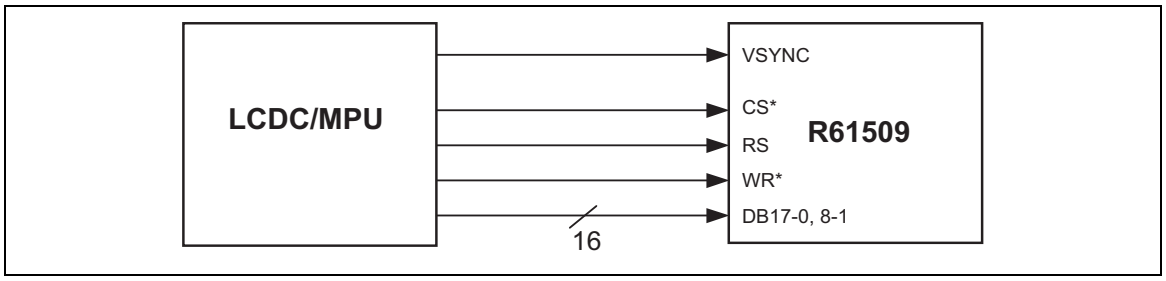


Figure 30 VSYNC Interface

The VSYNC interface is selected by setting DM1-0 = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display operation speed + margin), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the R61509 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display. By writing data using high-speed write function (HWM =1), the R61509 can write data via VSYNC interface in high speed with low power consumption.

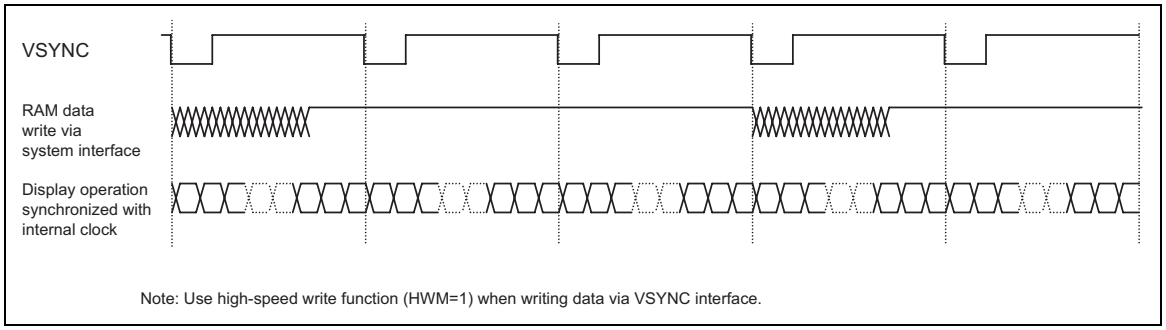


Figure 31 Moving Picture Data Transfers via VSYNC Interface

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$\begin{aligned}&\textit{Internal clock frequency (fosc) [Hz]}\\&= \textit{FrameFrequency} \times (\textit{DisplayLines(NL)} + \textit{FrontPorch(FP)} + \textit{BackPorch(BP)}) \times 23(\textit{clocks}) \times \textit{variance}\end{aligned}$$

$$\textit{RAMWriteSpeed(min.)[Hz]} > \frac{240 \times \textit{DisplayLines(NL)}}{(\textit{BackPorch(BP)} + \textit{DisplayLines(NL)} - \textit{margins}) \times 23(\textit{clocks}) \times \frac{1}{\textit{fosc}}}$$

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Panel size	240 RGB × 432 lines (NL = 6'h35: 432 lines)
Total number of lines (NL)	432 lines
Back/front porch	14/2 lines (BP = 4h'E, FP = 4'h2)
Frame frequency	60 Hz
Internal clock frequency	678 kHz

Internal clock frequency (fosc) [Hz]
= 678 kHz × 1.07 / 1.0 = 726 kHz

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±7% for variances and guarantee that display operation is completed within one VSYNC cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz]
> 240 × 432 / {((14 + 432 - 2) lines × 23 clocks) × 1/726 kHz} = 7.4 MHz

Notes: 1. In this example, it is assumed that the R61509 starts writing data in the internal RAM on the falling edge of VSYNC.
2. There must be at least a margin of 2 lines between the line to which the R61509 has just written data and the line where display operation on the LCD is performed.

In this example, the RAM write operation at a speed of 7.4 MHz or more, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the R61509 starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

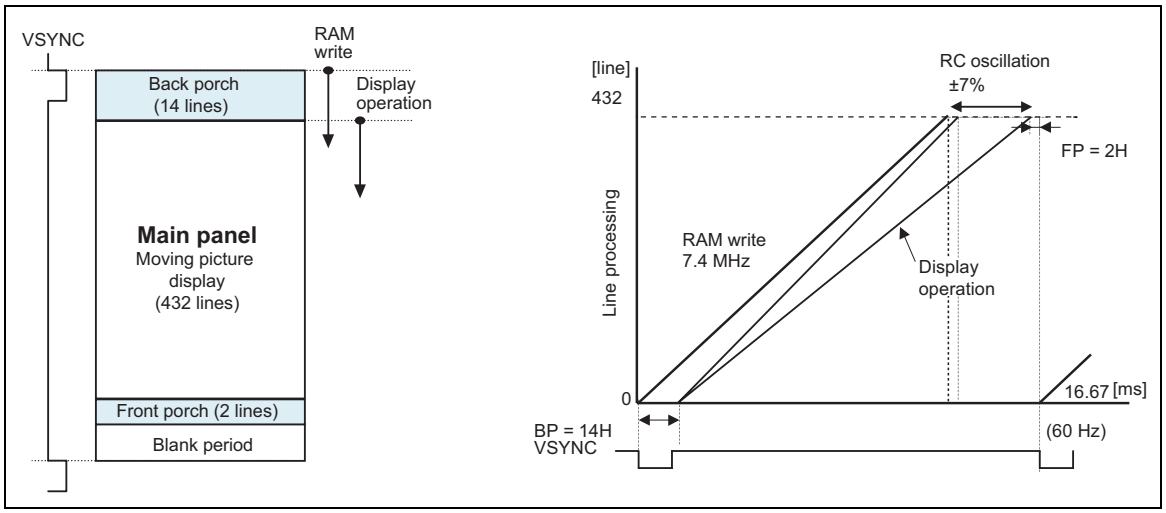


Figure 32 Write/Display Operation Timing via VSYNC Interface

Notes to VSYNC Interface Operation

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margins in setting RAM write speed for VSYNC interface operation.

2. The above example shows the values when writing over the full screen. Extra margin will be created if the moving picture display area is smaller than that.

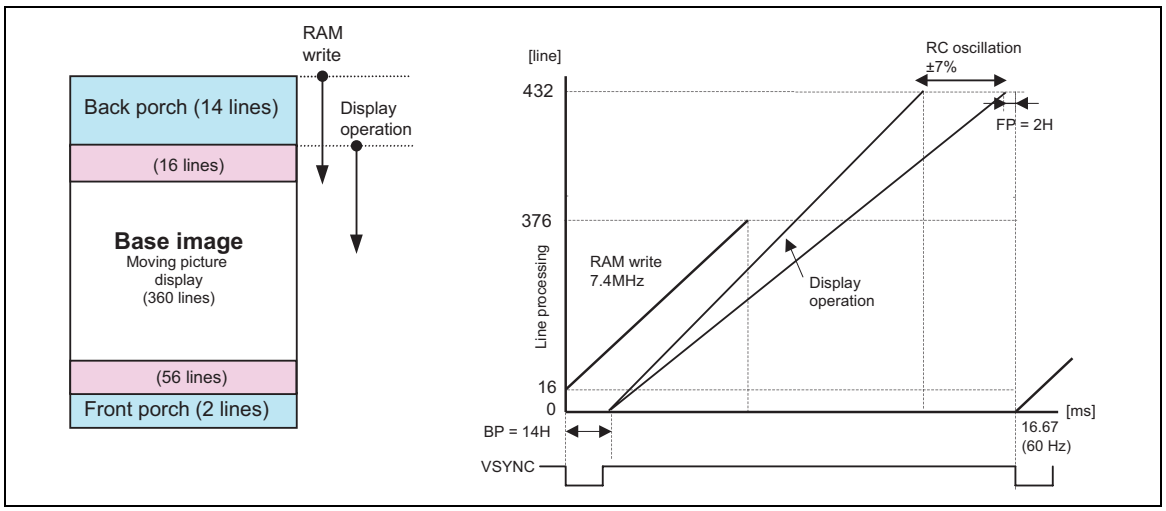


Figure 33 RAM Write Speed Margins

3. The front porch period continues from the end of one frame period to the next VSYNC input.
4. The instructions to switch from internal clock operation (DM1-0 = 00) to VSYNC interface operation modes and vice versa are enabled from the next frame period.
5. The partial display and vertical scroll functions are not available in VSYNC interface operation.
6. In VSYNC interface operation, set AM = 0 to transfer display data correctly.
7. In VSYNC interface operation, use high-speed write function (HWM = 1) when writing display data to the internal RAM.

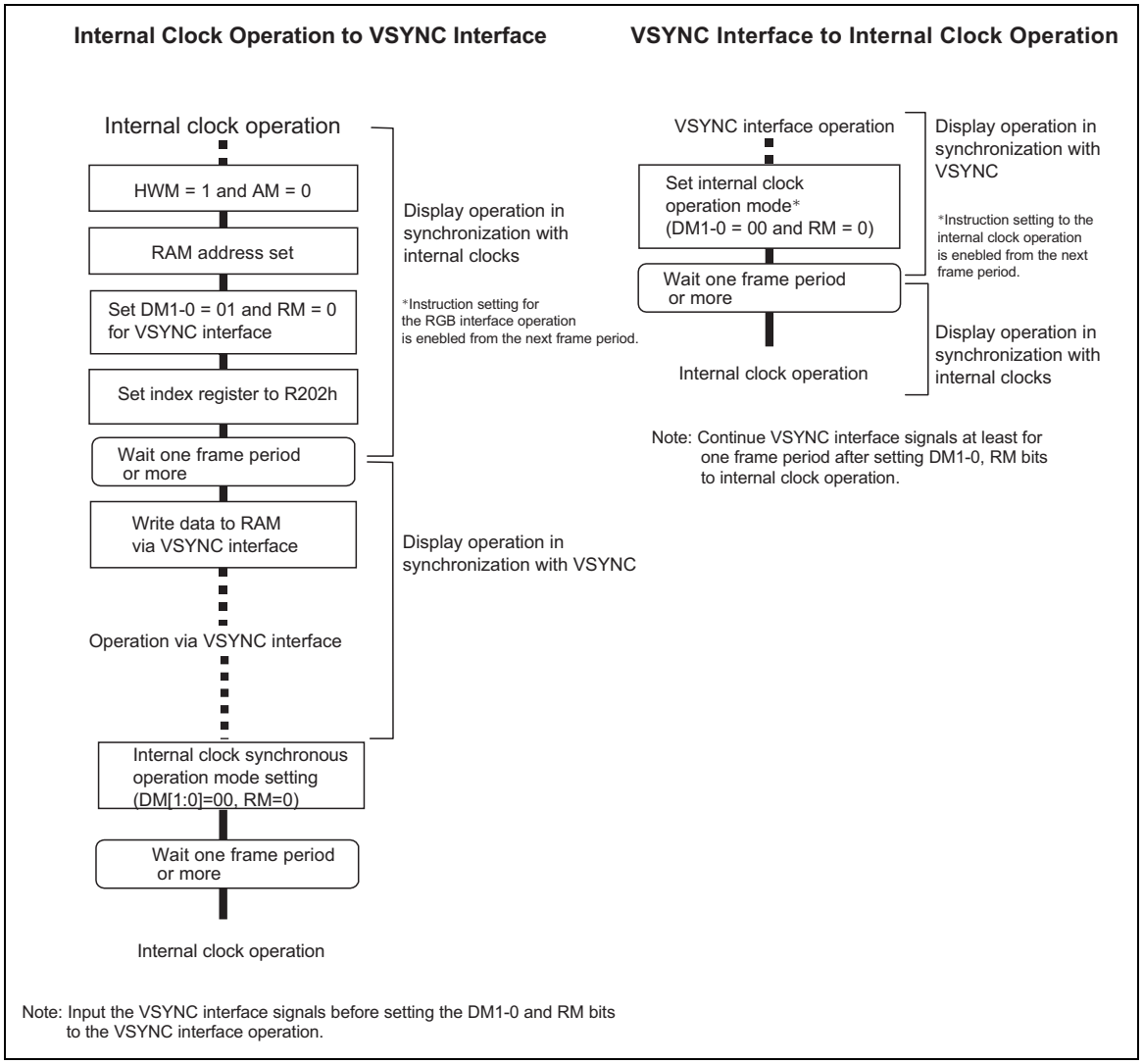


Figure 34 Sequences to Switch between VSYNC and Internal Clock Operation Modes

FMARK Interface

In the FMARK interface operation, data is written to internal RAM via system interface synchronizing with the frame mark signal (FMARK), realizing tearing less video image while using conventional system interface. FMARK output position is set in units of line using FMP bit. Set the bit considering data transfer speed.

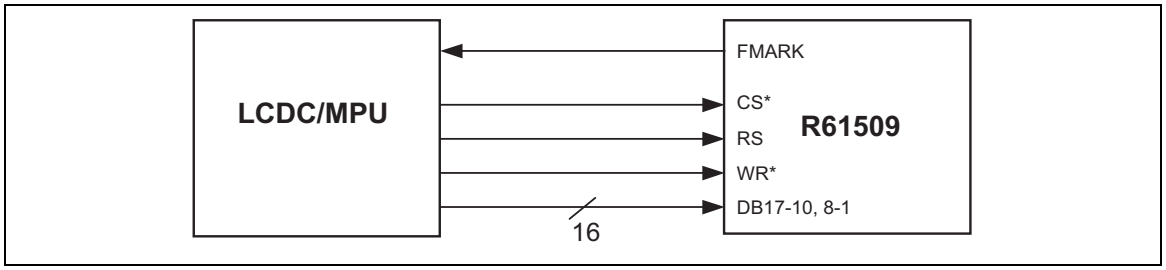


Figure 35 FMARK Interface

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture RAM area without causing flicker on the display.

The data is written in the internal RAM. Therefore, when moving picture is displayed, data is written only to the moving picture display area without using RGB or VSYNC interface, minimizing number of data transfer required for moving picture display. High-speed write function (HWM = 1) enables writing data in high speed with low power consumption.

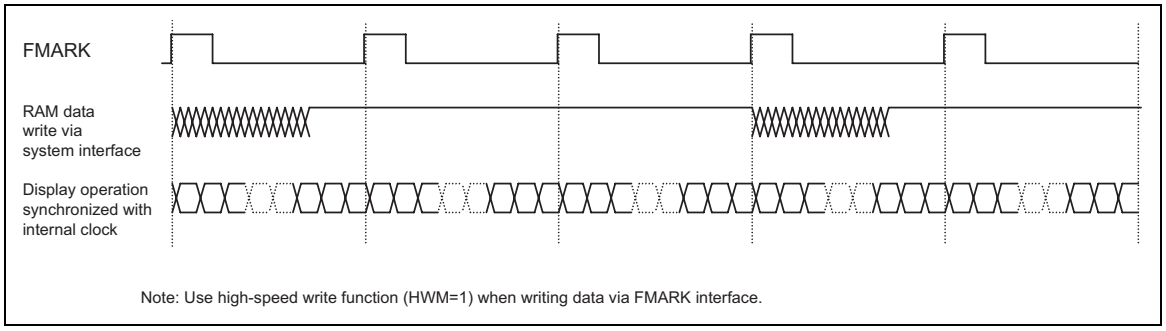


Figure 36 Moving Picture Data Transfers via FMARK function

When transferring data in synchronization with FMARK signal, minimum RAM data write speed and internal clock frequency must be taken into consideration. They must be more than the values calculated from the following equations.

$$\begin{aligned}&\text{Internal clock frequency (fosc) [Hz]}\\&= \text{FrameFrequency} \times (\text{DisplayLines}(NL) + \text{FrontPorch}(FP) + \text{BackPorch}(BP)) \times 23(\text{clocks}) \times \text{variance}\end{aligned}$$

$$\text{RAMWriteSpeed(min.)[Hz]} > \frac{240 \times \text{DisplayLines}(NL)}{(\text{FrontPorch}(FP) + \text{BackPorch}(BP) + \text{DisplayLines}(NL) - \text{margins}) \times 16(\text{clocks}) \times \frac{1}{fosc}}$$

Note: When RAM write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

Examples of calculating minimum RAM data write speed and internal clock frequency is as follows.

[Example]

Panel size	240 RGB × 432 lines (NL = 6'h35: 432 lines)
Total number of lines (NL)	432 lines
Back/front porch	14/2 lines (BP = 4h'E, FP = 4'h2)
Frame marker position (FMP)	Display end line: 432nd line (FMP = 9'h1BF)
Frame frequency	60 Hz
Internal oscillation frequency	678kHz

Internal oscillation frequency (fosc) [Hz] = 678kHz × 1.07 / 1.0 = 726 kHz (variance is taken into account)

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±7% for variances and guarantee that display operation is completed within one FMARK cycle.

2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz]
> 240 × 320 / {((2+14 + 320 – 2) lines × 16 clocks) × 1/726 kHz} = 7.4 MHz

Notes: 1. In this example, it is assumed that the R61509 starts writing data in the internal RAM on the rising edge of FMARK.

2. There must be at least a margin of 2 lines between the line to which the R61509 has just written data and the line where display operation on the LCD is performed.

3. The FMARK signal output position is set to the line specified by FMP[8:0] bits.

In this example, RAM write operation at a speed of 7.4MHz or more, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the R61509

starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

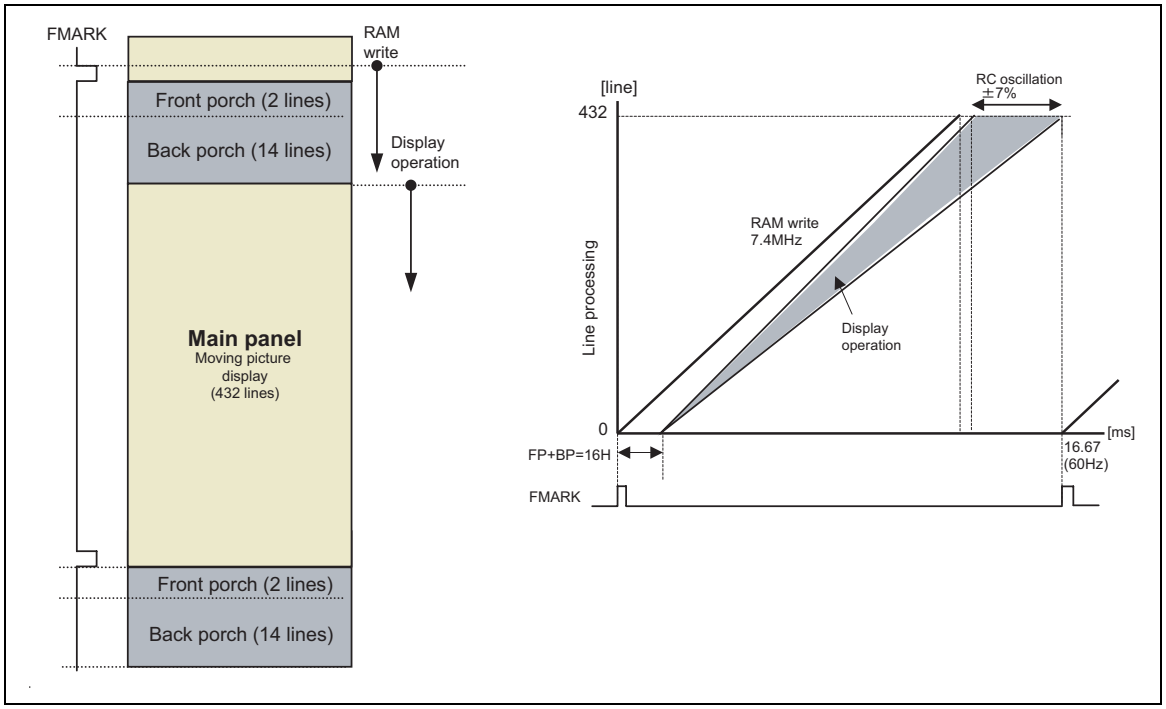


Figure 37

Notes to display operation synchronous data transfer using FMARK signal

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margin in setting RAM write speed for this operation.
2. Use high-speed write function (HWM = 1).

FMP bit setting

The microcomputer detects FMARK signal outputted at the position defined by FMP bit. The R61509 outputs an FMARK pulse when the R61509 is driving the line specified by FMP bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

The FMARK output interval is set by FMI bits. Set FMI bits in accordance with display data rewrite cycle and data transfer rate.

Table 74

FMP[8:0]	FMARK output position
9'h000	0
9'h001	1st line
9'h002	2nd line
:	
9'h1BD	445th line
9'h1BE	446th line
9'h1BF	447th line
9'h1C0 ~ 1FF	Setting disabled

Table 75

FMI[2]	FMI[1]	FMI[0]	FMARK Output interval
0	0	0	One frame period
0	0	1	2 frame periods
0	1	1	4 frame periods
1	0	1	6 frame periods
Other setting			Setting disabled

FMP setting example

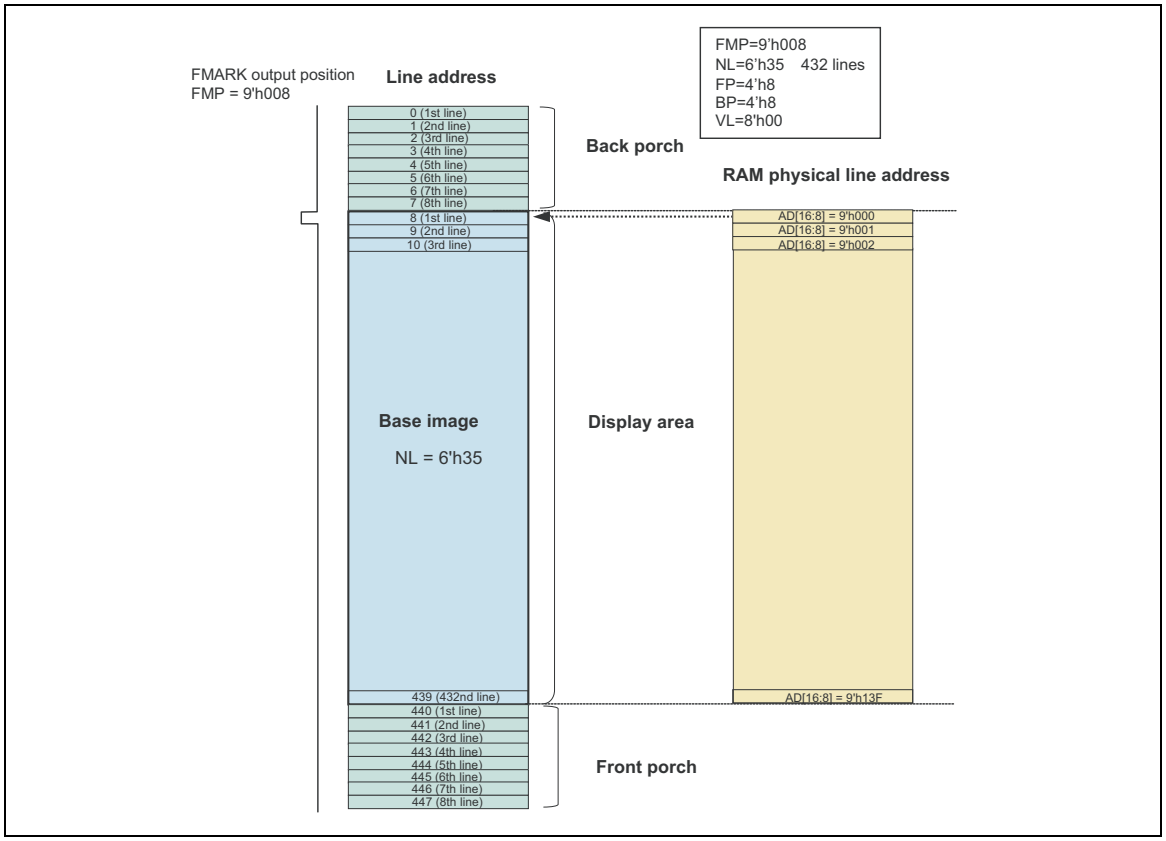


Figure 38

MDDI (Mobile Display Digital Interface)

MDDI (Mobile display digital interface) is a differential small amplitude serial interface for high-speed data transfer via following 4 lines: Stb+/- (MDDI_STBP_B, MDDI_STB_M_B), Data+/- (MDDI_DATA_P_B, MDDI_DATA_M_B).

The specifications of MDDI supported by the R61509 are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following is the specification MDDI supported by the R61509.

R61509's MDDI Specifications

- MDDI Type-I
- High-speed, differential, small-amplitude data transfer via Stb+/-, Data+/- lines
- MDDI client: the R61509 enables direct connection to the base band (BB) chip without bridge chip
- Cost-performance optimized interface for mobile display systems

1. Only internal mode (one client) and Forward Link are supported
2. Hibernation mode to save power consumption
3. Tearing-free moving picture display via FMARK/VSYNC interface
4. Moving picture display with low power consumption, realized by the features 2 ~ 3
5. Shutdown mode for saving power consumption in the standby state

Incorporates an output port for sub-display interface or peripheral control

Providing single-chip solution for MDDI mobile display systems

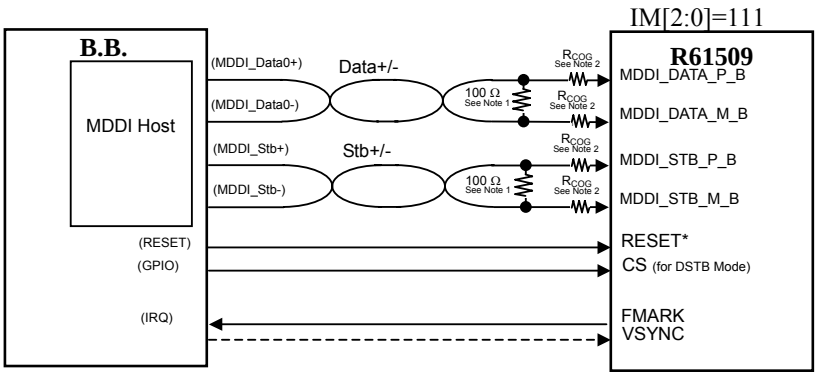


Figure 39

Notes: 1. An external end resistor of 100 ohm is necessary between Data+ and Data- lines
2. Make the COG wiring resistances of Data+/-, Stb+/- lines as small as possible (RCOG < 10 ohm).

MDDI Link Protocol (Packets Supported by the R61509)

The MDDI Link Protocol of the R61509 is in line with the MDDI specifications disclosed by VESA. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

The MDDI packets supported by the R61509 are as follows. Do not send packets not supported by the R61509 in the system incorporating the R61509.

Sub-Frame Header Packet

Bits	0	1	2	3	4	5	6	7
1	Packet Length							
2	(0x0014)							
3	Packet Type							
4	(0x3bff)							
5	Unique word							
6	(0x005a)							
7	Reserved1							
8	(0x0000)							
9	Sub-Frame Length							
10								
11								
12								
13	Protocol Version							
14	(0x0000)							
15	Sub-frame Count							
16								
17	Media-frame Count							
18								
19								
20								
21	CRC							
22								

Figure 40

Video Stream Packet

The R61509 writes image data to RAM via Video Stream Packet. The window and RAM addresses are set via Register Access Packet.

Bit	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0010)							
5	bClient ID							
6	(0x0000)							
7	Video Data Format Descriptor							
8								
9	Bit0	Bit1	Pixel Data Attributes					
10								
11	X Left Edge							
12								
13	Y Top Edge							
14								
15	X Right Edge							
16								
17	Y Bottom Edge							
18								
19	X Start							
20								
21	Y Start							
22								
23	Pixel Count							
24								
25	Parameter CRC							
26								
	Pixel Data (Packet Length: 26bytes)							
	Pixel Data CRC							

Note: The parameters colored in gray are not supported by the R61509.

Figure 41

Video Data Format Descriptor: sets the pixel data format. The R61509 supports only the following format. Set the same pixel format (bpp) as selected by DSS[1:0] in Video Data Format Descriptor.

Table 76

[15:13]	[12]	[11:8]	[7:4]	[3:0]	
010	1	0x5	0x6	0x5	Packed 16bpp RGB format (R:G:B=5:6:5)
010	1	0x6	0x6	0x6	Packed 18bpp RGB format (R:G:B=6:6:6)
Other					Setting disabled

Table 77

	MDDI byte n								MDDI byte n+1								MDDI byte n+2							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packed 16bpp	0	1	2	3	4	0	1	2	3	4	5	0	1	2	3	4	0	1	2	3	4	0	1	2
	Pixel1 Blue					Pixel1 Green						Pixel1 Red					Pixel2 Blue					Pixel2 Green		
Packed 18bpp	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
	Pixel1 Blue						Pixel1 Green						Pixel1 Blue						Pixel2 Blue					

Pixel Data Attributes: the image data sent vial Video Stream Packet is recognized as either the data for the main-panel or for the sub-panel according to the setting in [1:0] bits in this field.

Table 78

Pixel Data Attributes	Bits[1:0]	Description
0x0000	00	The Video Stream Packet data is recognized as the sub-panel data. The Video Stream Packet data is outputted via sub-display interface and not written in the R61509 see Note below
0x0001	01	Setting disabled
0x0002	10	Setting disabled
0x0003	11	The Video Stream Packet data is recognized as the data written in the R61509. The Video Stream Packet data is written in the R61509 and not outputted via sub-display interface.
Others		Setting disabled

Note: The following is the example of data transfer via Sub-display Video Stream Packet in RAM write operation via sub-display interface. Before transferring data to the sub display, the R61509 performs index write operation. The data is transferred only via 80-system 16-bit interface in one transfer per unit of data.

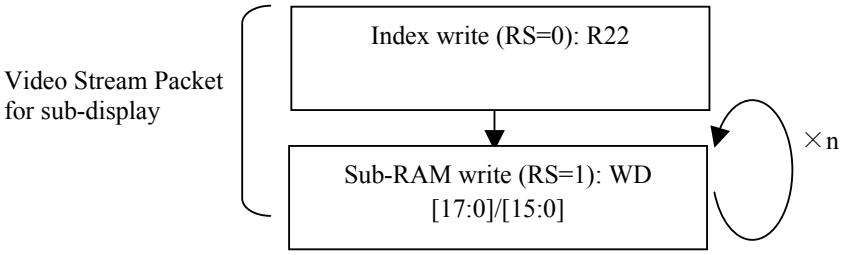
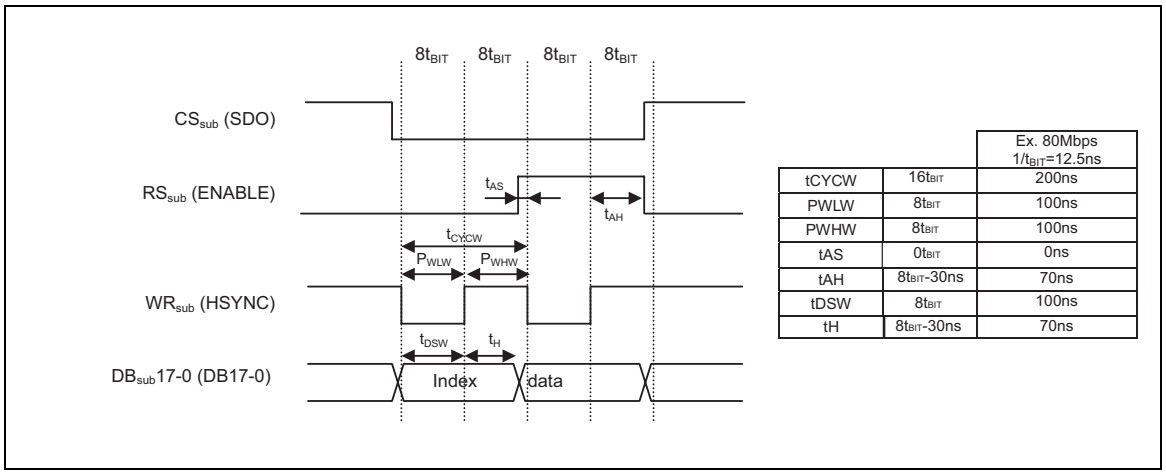


Figure 42 Sub-Display Interface RAM Write Sequence (18-/16-bit)

Table 79 Restrictions in Data Transfer via Video Stream Access Packet in RAM Write Operation via Sub-Display Interface

Sub-display interface	80-system 18-/ 16-bit interface, one transfer/unit of data
Video Data Format Descriptor	Packed 18/16 bpp
AM (bit) setting	0 (Horizontal write)
HWM (bit) setting	1 (Use high-speed write function)
RAM data write	Write data within a window address area in units of lines
RAM start address RAM window address	Set these addresses via Register Access Packet



		Ex. 80Mbps $1/t_{BIT}$=12.5ns
tCYCW	$16t_{BIT}$	200ns
PWLW	$8t_{BIT}$	100ns
PWHW	$8t_{BIT}$	100ns
tAS	$0t_{BIT}$	0ns
tAH	$8t_{BIT}$-30ns	70ns
tDSW	$8t_{BIT}$	100ns
tH	$8t_{BIT}$-30ns	70ns

Figure 43 Sub-Display Interface Timing

Register Access Packet

Register Access Packet is used when setting instruction to the R61509. Do not use this packet for RAM access.

Bit	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0092)							
5	bClient ID							
6	(0x0000)							
7	Read/Write Info							
8								
9	Register Address							
10								
11								
12								
13	Parameter CRC							
14								
	Register Data List (Packet Length: 14bytes)							
	Register Data CRC							

Note: The parameters colored in gray are not supported by the R61509.

Figure 44

Read/Write Info: Read or Write information in register access. The R61509 supports only the following access setting.

Table 80

Bits[15:14]	Bits[13:0]	Function
00	0x0001	Single Access mode, in which one instruction is set via one register access packet
00	0xn	In multi random access mode, the number of Register Data (index+instruction) is set.
Other		Setting disabled.

Register Address: The index of the register to be accessed is set in Register Address area. Also, the register access mode, i.e. single or multi random access mode, and whether the Register Address Packet is directed to the R61509 or the sub display are determined by the setting in Register Address area.

Table 81

Bit[31]	Function
0	Single Access mode. The index of the register to be accessed (ID[11:0]) is set in bits[11:0] in Register Address. The instruction set (IB[15:0]) to be written in the register is stored in the Register Data area in Register Access Packet.
1	Multi Random Access mode. The index of the register to be accessed (ID[11:0]) is stored in the upper 2 bytes in the Register Data area in Register Access Packet. The instruction set (IB[15:0]) to be written in the register is stored in the lower 2 bytes in the Register Data area in Register Access Packet. In Multi Random Access mode, both index and instruction set are stored in the Register Data area and instruction set can be transferred consecutively without setting the index in Register Address in each time transferring instruction.

Table 82

Bit[30:12]	Function
19'h00000	The Register Access Packet is directed to the R61509 via main-display interface.
19'h00001	The Register Access Packet is directed to the sub display via sub-display interface.
19'h00002 ~ 19'h7FFFF	Setting disabled.

Table 83

Bit[11:0]	Function
Single Access	Bits [11:0] are used as index [11:0].
Multi Random Access	In Multi Random Access mode, bits [11:0] are not used. Set "0" to all bits.

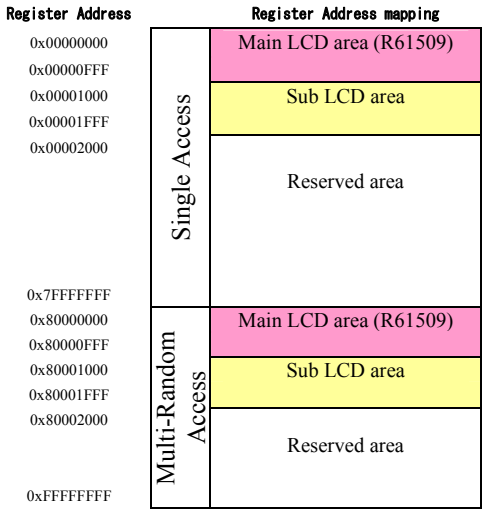


Figure 45 Register Address Area (Write Mode, Main/Sub Area)

Register Data: The data for register access is written in Register Data. Four bytes are allocated for one instruction.

Table 84

Bits[31:16]	Bits[15:0]	Function
All 0	Instruction IB[15:0]	In Single access mode, the instruction set written in bits[15:0] is set in the register, which is specified in the bits[11:0] in Register Address.
4h0 + Index ID[11:0]	Instruction IB[15:0]	In Multi Random Access mode, both index and instruction set are stored in Register Data to allow consecutive instruction setting without setting the index in Register Address in each time transferring instruction.

Example of Register Access Packet in Single Access mode (e.g. write to the R61509)

	0	1	2	3	4	5	6	7
1	Packet Length					(0x12)		
2						(0x00)		
3	Packet Type					(0x92)		
4						(0x00)		
5	bClient ID					(0x00)		
6						(0x00)		
7	Read/Write Info					(0x01)		
8						(0x00)		
9	Register Address				(index ID[7:0])			
10					(0x0, upper index ID[11:8])			
11						(0x00)		
12						(0x00)		
13	Parameter CRC							
14								
15	Register Data List				(Lower instruction IB[7:0])			
16					(Upper instruction IB[15:8])			
17						(0x00)		
18						(0x00)		
19	Register Data CRC							
20								

Note: The parameters colored in gray are not supported by the R61509.

Figure 46

Example of Register Access Packet in Multi Random Access mode (e.g. write 4 instructions to the R61509)

	0	1	2	3	4	5	6	7
1	Packet Length					(0x1E)		
2						(0x00)		
3	Packet Type					(0x92)		
4						(0x00)		
5	bClient ID					(0x00)		
6						(0x00)		
7	Read/Write Info					(0x04)		
8						(0x00)		
9	Register Address					(0x00)		
10					(0x00)	*0x10: sub display		
11						(0x00)		
12						(0x80)		
13	Parameter CRC							
14								
15	Register Data List 1st index+instruction					(Lower instruction IB1[7:0])		
16						(Upper instruction IB1[15:8])		
17						(Lower index ID1[7:0])		
18						(Upper index ID1[15:8])		
19	2nd index+instruction					(Lower instruction IB2[7:0])		
20						(Upper instruction IB2[15:8])		
21						(Lower index ID2[7:0])		
22						(Upper index ID2[15:8])		
23	3rd index+instruction					(Lower instruction IB3[7:0])		
24						(Upper instruction IB3[15:8])		
25						(Lower index ID3[7:0])		
26						(Upper index ID3[15:8])		
27	4th index+instruction					(Lower instruction IB4 [7:0])		
28						(Upper instruction IB4 [15:8])		
29						(Lower index ID4 [7:0])		
30						(Upper index ID4 [15:8])		
31	Register Data CRC							
32								

Note: The parameters colored in gray are not supported by the R61509.

Figure 47

Register Access Packet Restrictions

The R61509's internal RAM is accessible via Video Stream Packet. RAM access data is not included in Register Access Packet.

Link Shutdown Packet

This packet is used to bring Link to the Hibernation state.

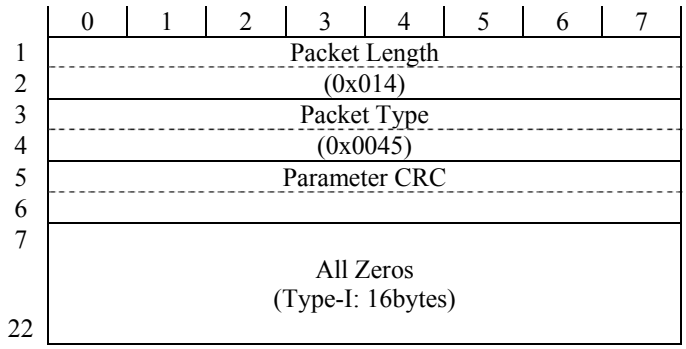


Figure 48

Filler Packet

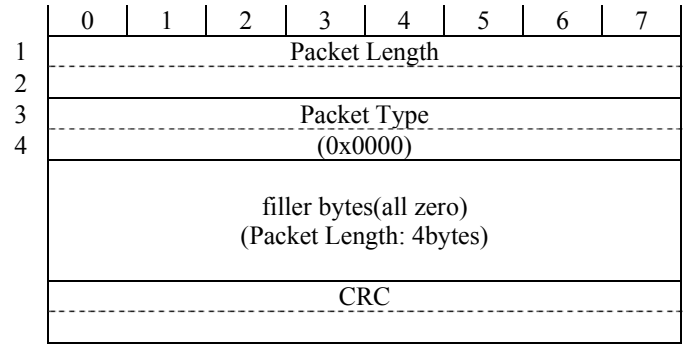


Figure 49

MDDI Instruction Setting

Instruction Setting in Single Access Mode

In Single Access mode, one instruction set is transferred in one Register Access Packet. When transferring a multiple number of instruction sets, they must be transferred in the same number of Register Access Packets.

Table 85

Register Access Packet Parameter	Register Setting
Read/Write Info[15:0]	0 x 0001
Register Address[31:0]	20'h0000000+ID[11:0]
Register Data[31:0]	16'h0000+IB[15:0]

MDDI Packet
sRAP(x,y) = Single Register Access Packet (ID[15:0], IB[15:0])

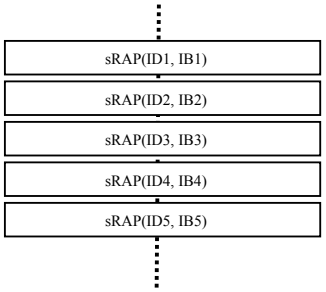


Figure 50

Instruction Setting via Multi Random Access Mode

In Multi Random Register Access operation, both index and instruction set are stored in one field of Register Data List in the Register Access Packet to allow random instruction setting. In this mode, a multiple number of instruction sets can be transferred in one Register Access Packet.

Table 86

Register Access Packet Parameter	Register Setting
Read/Write Info[15:0]	0 x n (n: Number of Register List)
Register Address[31:0]	32'h8000_0000
Register Data List[31:0]	ID[15:0] + IB[15:0]

MDDI Packet
mRAP(x,y) = Multi-random Register Access Packet (ID[15:0],IB[15:0])

Figure 51

RAM Access Setting Example

The following are examples of RAM access via Video Stream Packet and register access via Register Access Packet in Single and Multi Random Access modes.

Example: 240RGB x 432 panel, full screen rewrite, 18bpp data

MDDI Packet: Single Access Mode

sRAP (x, y) = Register Access Packet (ID[15:0], IB[15:0]) in Single Access Mode
VSP (p, n) = Video Stream Packet (pixel data)

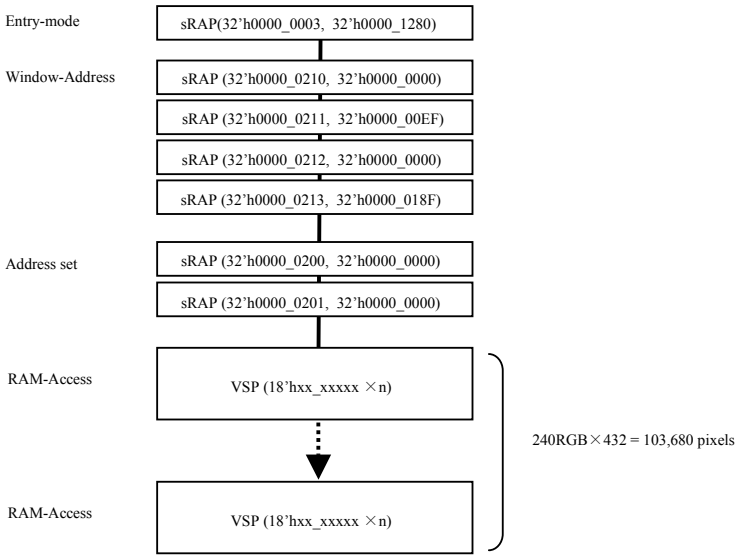


Figure 52

MDDI Packet: Multi Random Access Mode

mRAP (x, y) = Register Access Packet (ID[15:0], IB[15:0]) in Multi Random Access mode
VSP (p, n) = Video Stream Packet (pixel data)

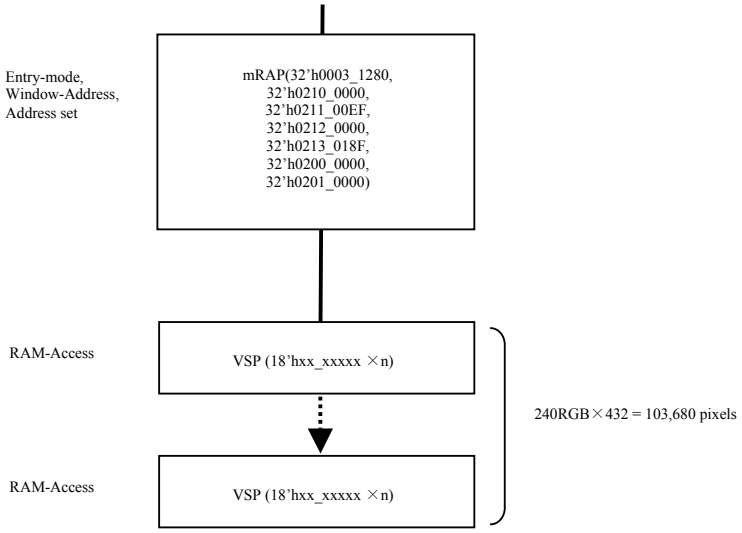


Figure 53

Table 87 Video Stream Access Packet Restriction

AM	0 (Horizontal write)
HWM	1 (High-speed write)
Data write transfer to RAM	Transfer data for each line at a time within the window address area
RAM start address **RAM window address**	Set them via Register Access Packet.

Table 88 Register Access Packet Restriction

RAM access	The R61509's internal RAM is accessible via Video Stream Packet. RAM access data is not included in Register Access Packet.

Hibernation Setting

The R61509's Client MDDI supports Hibernation setting. There are two ways to cancel the Hibernation setting, which can be selected according to the condition of use.

Table 89 Hibernation Cancellation

Cancel	Condition
Host-Initiated Wake up	In power-saving mode such as standby
FMARK-Initiated Wake up	Save power consumption in transferring moving picture data Host-initiated Wake up triggered by the output from FMARK

The Hibernation setting and cancellation sequence must be compatible with the VESA-MDDI specifications.

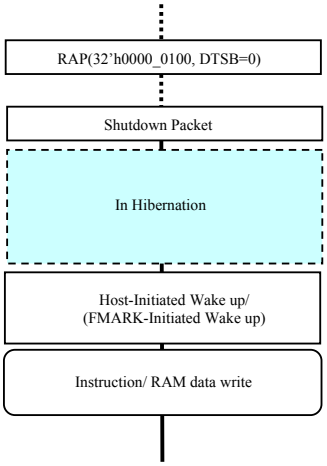


Figure 54

Shutdown Mode Setting

The R61509's Client MDDI supports shutdown setting to bring the R61509 to the standby state to save power consumption during Hibernation.

By setting DSTB = 1 and sending Shutdown Packet, MDDI enters the Hibernation state. The Client MDDI's standby power requirement can be reduced while MDDI Link is maintained in the Hibernation state.

In shutdown mode, the R61509 halts operation other than maintaining Hibernation state. In canceling shutdown mode, input Low pulse 6 times from CS pin. After canceling shutdown mode, cancel the Hibernation state by Host-initiated Wake up.

In shutdown mode, instruction setting and RAM data are not retained and they must be reset after canceling the Hibernation state.

When setting and canceling the Hibernation state, follow the sequence as specified in the MDDI specifications by VESA.

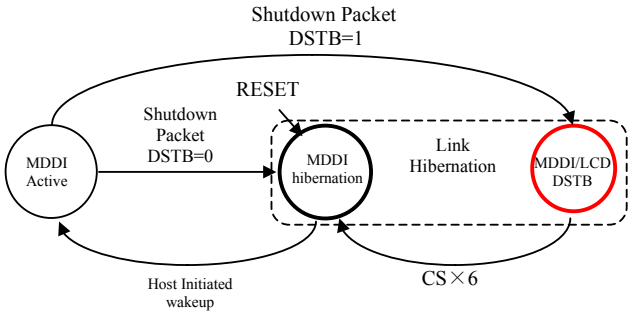


Figure 55 State Transitions in Shutdown Mode

Shutdown Mode Sequence

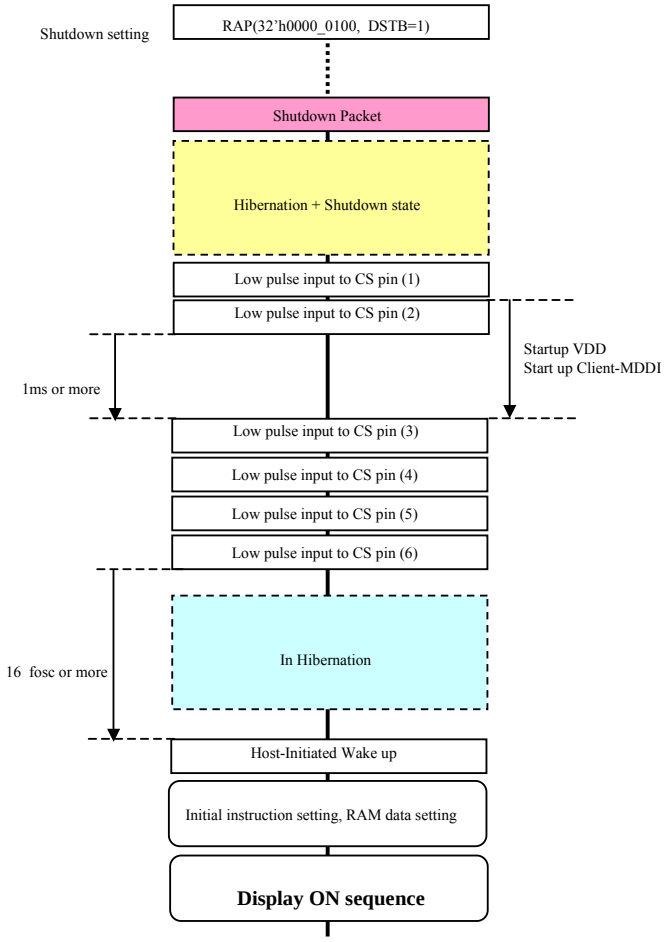


Figure 56

Note: In MDDI operation, the CS pin is used only for canceling the shutdown mode.

MDDI Moving Picture Interface

The R61509 supports FMARK and VSYNC interfaces to display moving picture in MDDI operation. Select either one according to the configuration of the system. By transferring data according to the following sequences, the R61509 can display moving picture via MDDI without tearing.

MDDI-FMARK Interface

The Client MDDI supported by the R61509 adopts 2-frame data transfer format when writing moving picture data. By synchronizing the moving picture data rewrite operation via MDDI with the frame mark signal from the R61509 (FMARK), the R61509 can display moving picture via MDDI without tearing.

The output position of FMARK can be changed in units of lines by setting FMP[8:0]. The output cycle of FMARK can also be changed in units of frames by setting FMI[2:0]. Make these settings according to the MDDI transfer speed and data rewrite cycle.

In combination with the Hibernation setting, moving picture can be displayed via MDDI-FMARK with low power consumption.

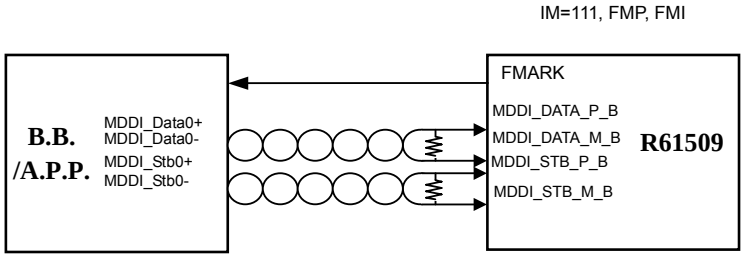


Figure 57

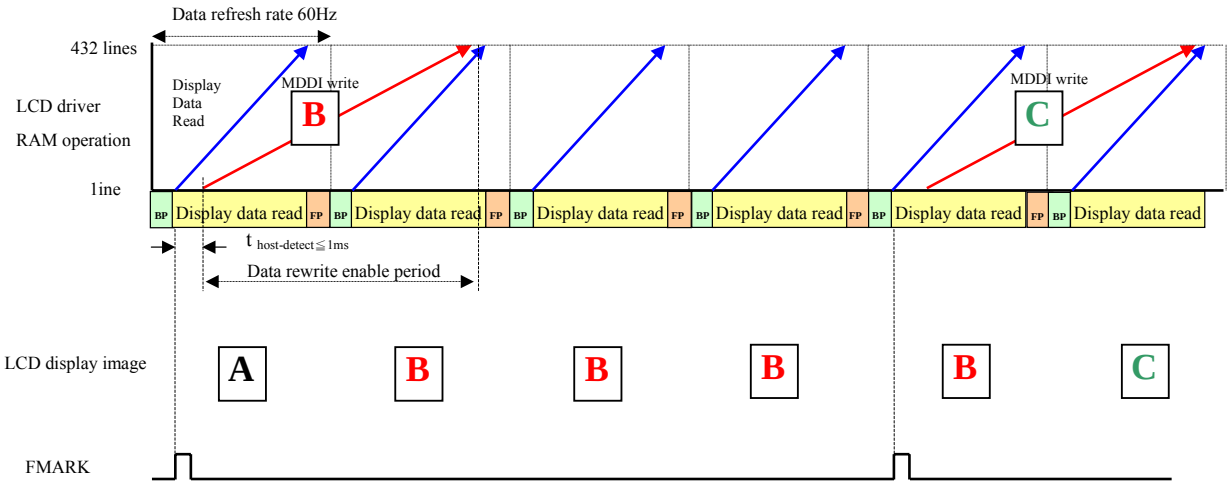


Figure 58

There are restrictions in setting the data transfer speed and internal oscillation frequency for MDDI data transfer to prevent tearing on the moving picture display. The RAM data write operation via MDDI must

be performed with the data transfer speed and the internal oscillation frequency calculated from the following formulas.

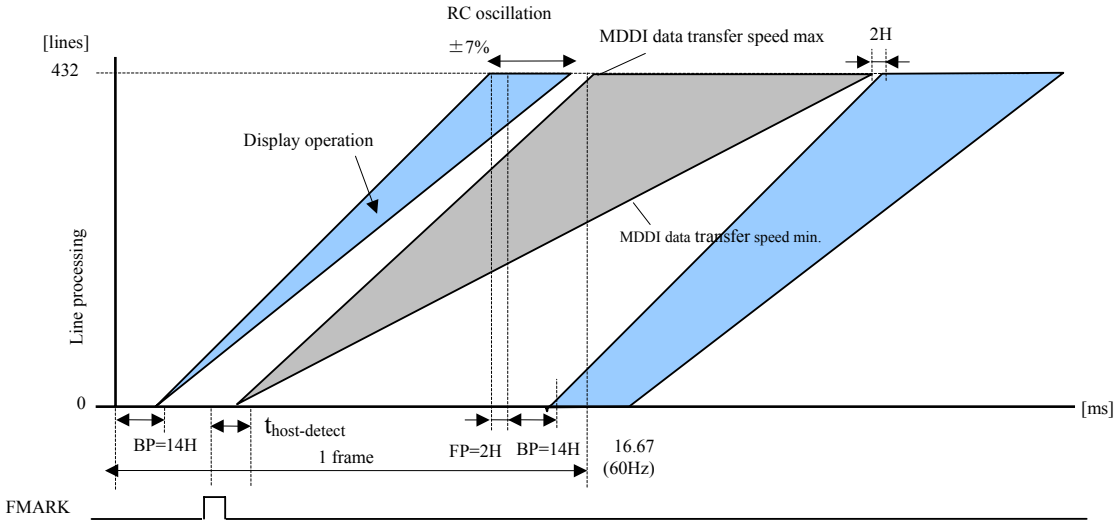


Figure 59

$$\textit{Internal clock frequency } (f_{osc}\,\max.)\ [Hz]$$
$$= FrameFrequency(f_F) \times (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) \times 16(clocks) \times \mathrm{variance}$$

$$TotalNumberOfDataTransfer$$
$$= (SubFrameHeaderPacket) \times 8(bits) + \frac{image\_Ysize}{BlockSize} \times 28(bytes) \times 8(bits) + (image\_Xsize \times image\_Ysize \times bpp)$$

$$MDDIdataTransferSpeed(\min.)[Mbps]$$
$$> \frac{TotalNumberOfDataTransfer}{((BP + NL + FP + BP + NL) - FMARKposition(FMP) - margins) \times RTN \times \frac{1}{f_{osc}\,\max.} - t_{host-detect}}$$

$\therefore MDDIdataTransferSpeed(min.) < MDDIdataTransferSpeed \leq 85Mbps$

Note: If the RAM write operation does not start on the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into consideration.

The following is an example of calculating MDDI data transfer speed and internal oscillation frequency for writing WQVGA full-screen moving picture data in synchronization with FMRAK without tearing.

Calculating Internal Oscillation Frequency f_{osc}

Display size: 240 RGB × 432 lines (NL0 = 432 lines)
Back/front porch: 14/2 lines (BP = 14/ FP = 2)
Line clock number (RTN): 23 clocks (RTNI = 17)
Frame frequency (f_F): 60 Hz
Internal oscillation frequency: 678kHz

$$\therefore InternalOscillationFrequency(f_{osc}\ \max.) = 678(Hz) \times \frac{1.07}{1.0} = 726(kHz)$$

Notes: 1. When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±7% for variances and ensures completion of display operation within one frame cycle (60Hz).

2. In this example, variances attributed to fabrication process of LSI and room temperature are taken into consideration. Other possible causes of variances, such as voltage changes, are not in consideration. It is necessary to include a margin for these factors if any.

Calculating Total Data to be Transferred per Frame

Display size: 240 RGB × 432 lines (image_X size = 240, image_Y size = 432)
Bit per pixel of image data: 18 bpp

$$\therefore TotalDataTransferred[bits] = 22(bytes) \times 8(bits) + \frac{432}{16} \times 28(bytes) \times 8(bits) + (240 \times 432 \times 18) = 1{,}872{,}464(bits)$$

Calculating MDDI Data Transfer Speed (min.)

FMARK output timing: 14 lines (FMP = 14)
Margins: 2 lines
Hibernation startup time ($t_{host\text{-}detect}$): 1 ms ($t_{host\text{-}detect}$ = 1ms)

$$\therefore MDDIdataTransferSpeed(\min.) = \frac{1{,}872{,}464(bits)}{(14 + 432 + 2 + 14 + 432 - 14 - 2) \times 23(clocks) \times \frac{1}{726(kHz)} - 1(ms)} = 70(Mbps)$$

MDDI-VSYNC Interface

The Client MDDI supported by the R61509 adopts 2-frame data transfer method in writing moving picture data. By synchronizing rewrite operation of moving picture data via MDDI with a frame synchronous signal from the system (VSYNC), the R61509 can display moving picture without tearing.

The R61509 operates in synchronization with the VSYNC signal from the system, which determines the frame cycle. The VSYNC signal must be supplied to the R61509 throughout the MDDI-VSYNC operation.

In combination with the Hibernation setting, the R61509 can display moving picture via MDDI-VSYNC interface with low power consumption.

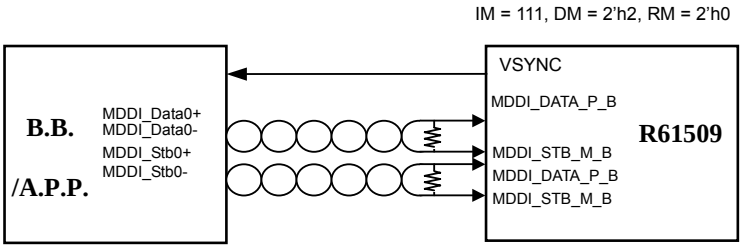
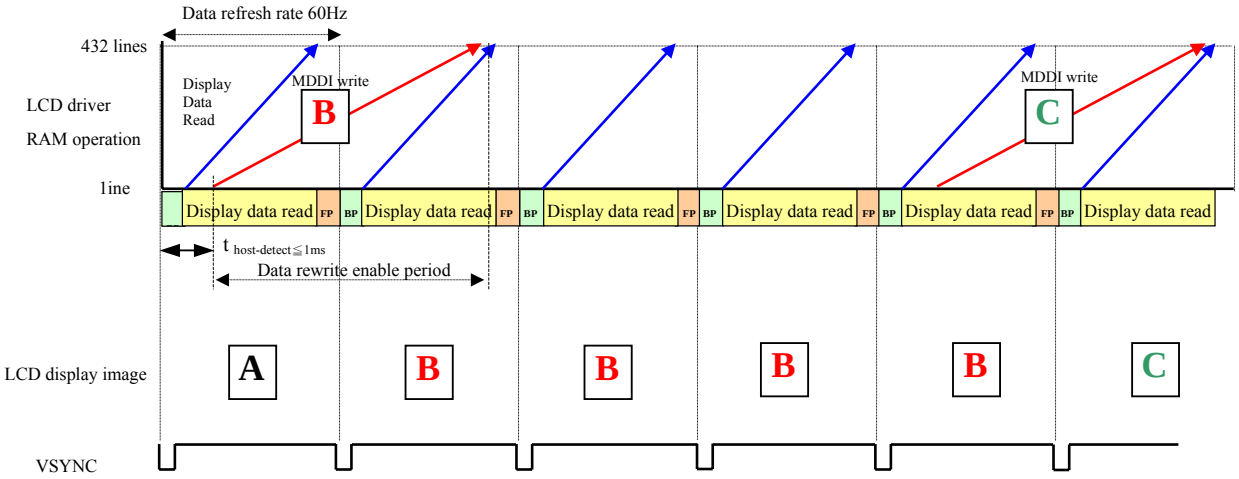


Figure 60



Note: The front porch (FP) period continues until next VSYNC input is detected.

Figure 61

There are restrictions in setting data transfer speed and internal oscillation frequency for MDDI data transfer to prevent tearing on moving picture display. The RAM data write operation via MDDI must be performed with the data transfer speed and the internal oscillation frequency calculated from the following formulas.

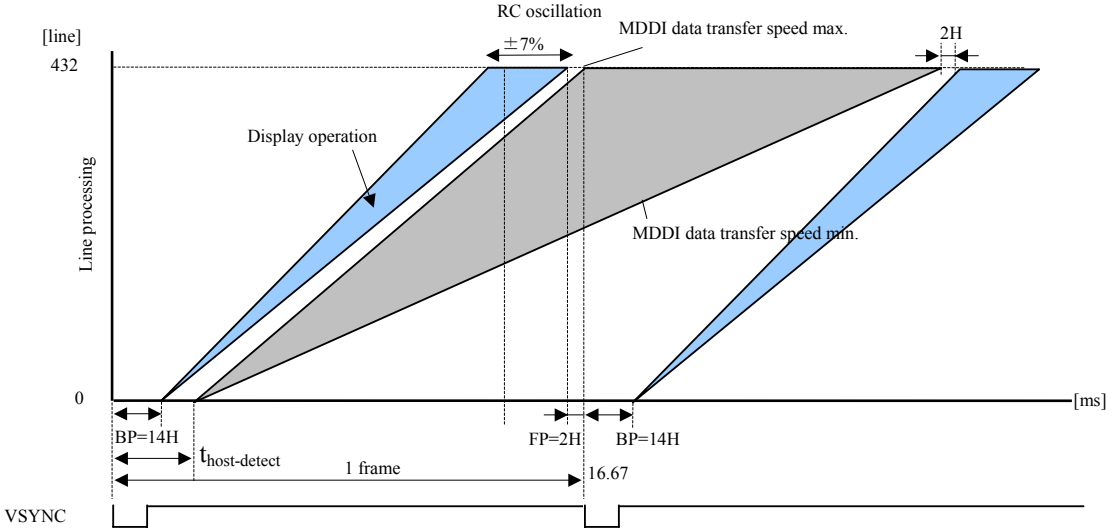


Figure 62

Internal clock frequency (f_{osc} max.) [Hz]

$$= FrameFrequency(f_{VSYNC}) \times (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) \times 23(clocks) \times variance$$

$$TotalNumberOfDataTransfer$$

$$= (SubFrameHeaderPacket) \times 8(bits) + \frac{image\_Ysize}{BlockSize} \times 28(bytes) \times 8(bits) + (image\_Xsize \times image\_Ysize \times bpp)$$

$$MDDIdataTransferSpeed(\min.)[Mbps] > \frac{TotalNumberOfDataTransfer}{\frac{1}{FrameFrequency(f_{VSYNC})} + (BP + NL - m\arg ins) \times RTN \times \frac{1}{f_{osc}\max.} - t_{host-detect}}$$

Here, BP <$t_{host\text{-}detect}$

$$\therefore MDDIdataTransferSpeed(min.) < MDDIdataTransferSpeed \le 85Mbps$$

Note: When the RAM write operation does not start on the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into consideration.

The following is an example of calculating MDDI data transfer speed and internal oscillation frequency in writing QVGA full-screen moving picture data in synchronization with VSYNC without tearing.

Calculating Internal Oscillation Frequency f_{osc}

Display size: 240 RGB × 432 lines (NL0 = 432 lines)
Back/front porch: 14/2 lines (BP = 14/ FP = 2)
Line clock cycle (RTN): 23 clocks (RTNI=17)
Frame frequency (f_{VSYNC}): 60 Hz

$$\therefore InternalOscillationFrequency(f_{osc}\ \max.) = 678(Hz) \times \frac{1.07}{1.0} = 726(kHz)$$

Notes: 1. When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±7% for variances and ensures completion of display operation within one frame cycle (60Hz).
2. In this example, variances attributed to fabrication process of LSI and room temperature are taken into consideration. Other possible causes of variances, such as voltage changes, are not in consideration. It is necessary to include a margin for these factors if any.

Calculating Total Data to be Transferred per Frame

Display size: 240 RGB × 432 lines (image_X size = 240, image_Y size = 432)
Bit per pixel of image data: 18bpp

$$\therefore TotalDataTransferred\ [bits] = 22(bytes) \times 8(bits) + \frac{432}{16} \times 28(bytes) \times 8(bits) + (240 \times 432 \times 18) = 1{,}872{,}464(bits)$$

Calculating MDDI Data Transfer Speed (min.)

Frame frequency ((fVSYNC): 60Hz
Back porch: 14 lines (BP =14)
Margins 2 lines
Hibernation startup time ($t_{host\text{-}detect}$): 1 ms ($t_{host\text{-}detect}$ = 1ms)

$$\therefore MDDIdataTransferSpeed(\min.) = \frac{1{,}872{,}464(bits)}{\frac{1}{60(Hz)} + (14 + 432 - 2) \times 23(clocks) \times \frac{1}{726(kHz)} - 1(ms)} = 63(Mbps)$$

MDDI Sub-Display Interface

The R61509 uses the 80-system 18/16-bit interfaces as the sub-display interface to allow controlling sub display and data write operation to the sub display via MDDI.

Sub-Display Interface Specifications

1. 80-system 18-/16-bit interfaces (one transfer per unit of data)
2. Transfer index ID[11:0] and instruction IB[15:0]
3. Compatible to 18-/16-bpp display

Sub-Display Interface Pin

In MDDI operation (IM = 111), the SDO, ENABLE, HSYNC, and the DB17-0 pins are used as the sub-display interface pin.

●When sub LCD driver has 80-system 18-bit interface

Table 90

R61509 Sub Display Interface Pin	Sub LCD Driver Connection (e.g. HD66791)
SDO	CS pin
ENABLE	WR pin
HSYNC	RS pin
DB17-0	DB17-0 pins

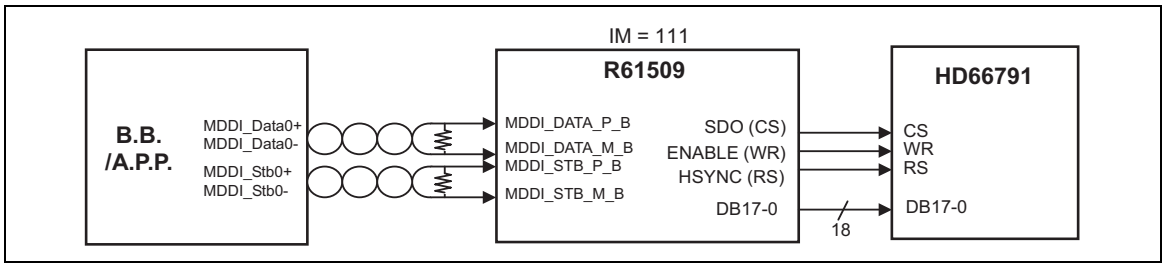


Figure 63

●When sub LCD driver has 80-system 16-bit interface

Table 91

R61509 Sub Display Interface Pin	Sub LCD Driver Connection (e.g. HD66791)
SDO	CS pin
ENABLE	WR pin
HSYNC	RS pin
DB17-10, 8-1	DB17-10, 8-1 pins

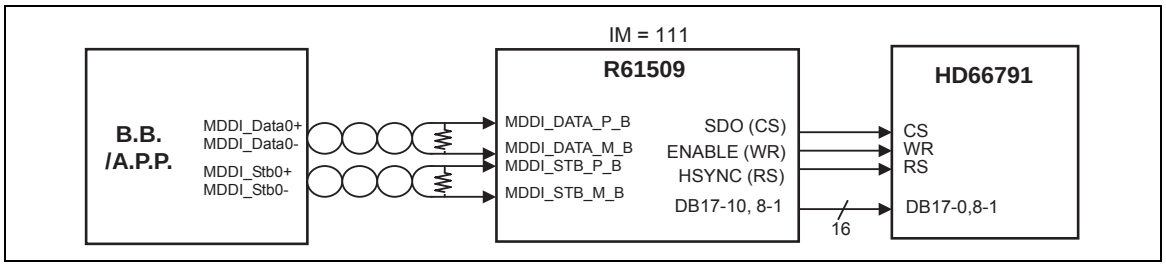


Figure 64

Sub-Display Interface Control

The sub display is controlled and the instruction is sent via MDDI packet. See MDDI Link Protocol (Packets Supported by the R61509).

Register Access Packet: The instructions sent to main and sub display are discerned by the field in Register Access Packet.

Video Stream Packet: Whether the data is transferred to main or sub display is discerned by the Pixel Attributes Bits[1:0]

MDDI Mobile Display System

The R61509 supports sub-display interface in order to coordinate the operation via MDDI. By bypassing the FML signal sent from the sub display, the R61509 realizes moving picture display on both main and sub panels via MDDI.

These features of R61509 enables configuration of MDDI mobile display system without adding bridge chip and so on.

R61509 MDDI Mobile Display System Configuration Example (16 bpp on sub display)

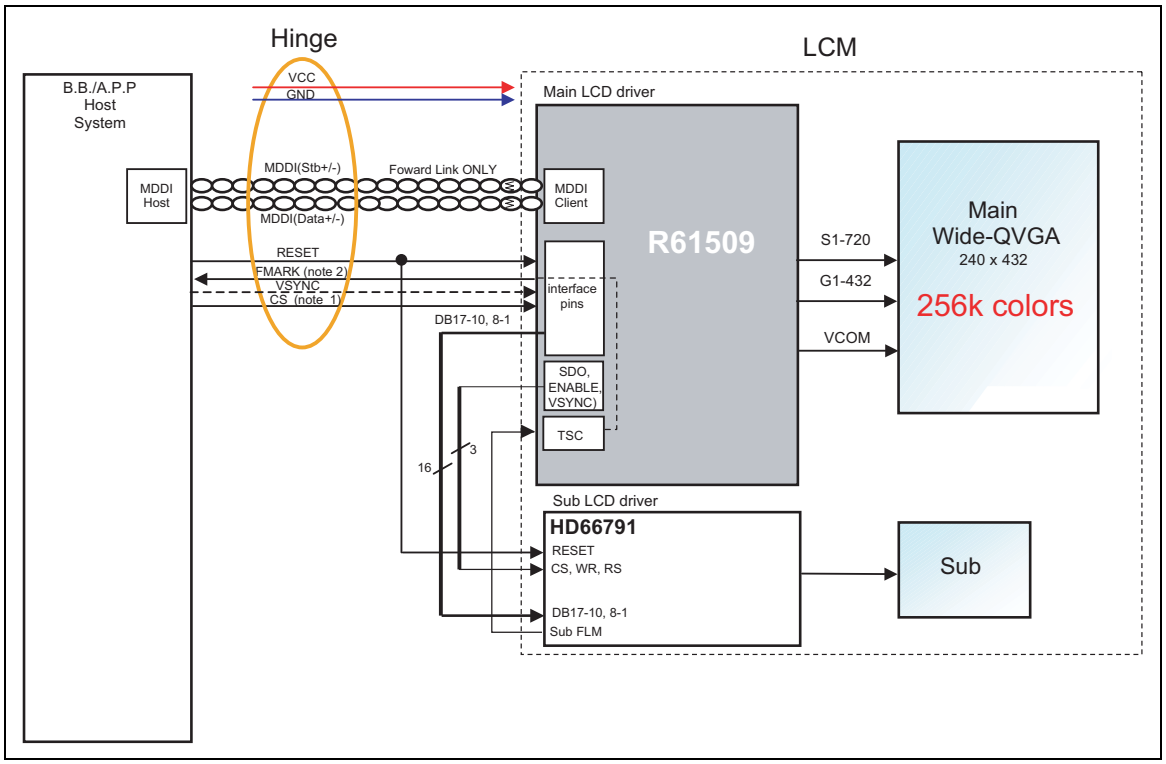


Figure 65

Notes: 1. The CS pin is used exclusively for the signal to cancel shutdown mode in MDDI operation. While not using Shutdown mode, the CS pin does not have to be connected to the Host System.

2. Use either FMARK or VSYNC signal as the reference signal for moving picture display according to the configuration of system.

RGB Interface

The R61509 supports the RGB interface. The interface format is set by RM[1:0] bits. The internal RAM is accessible via RGB interface.

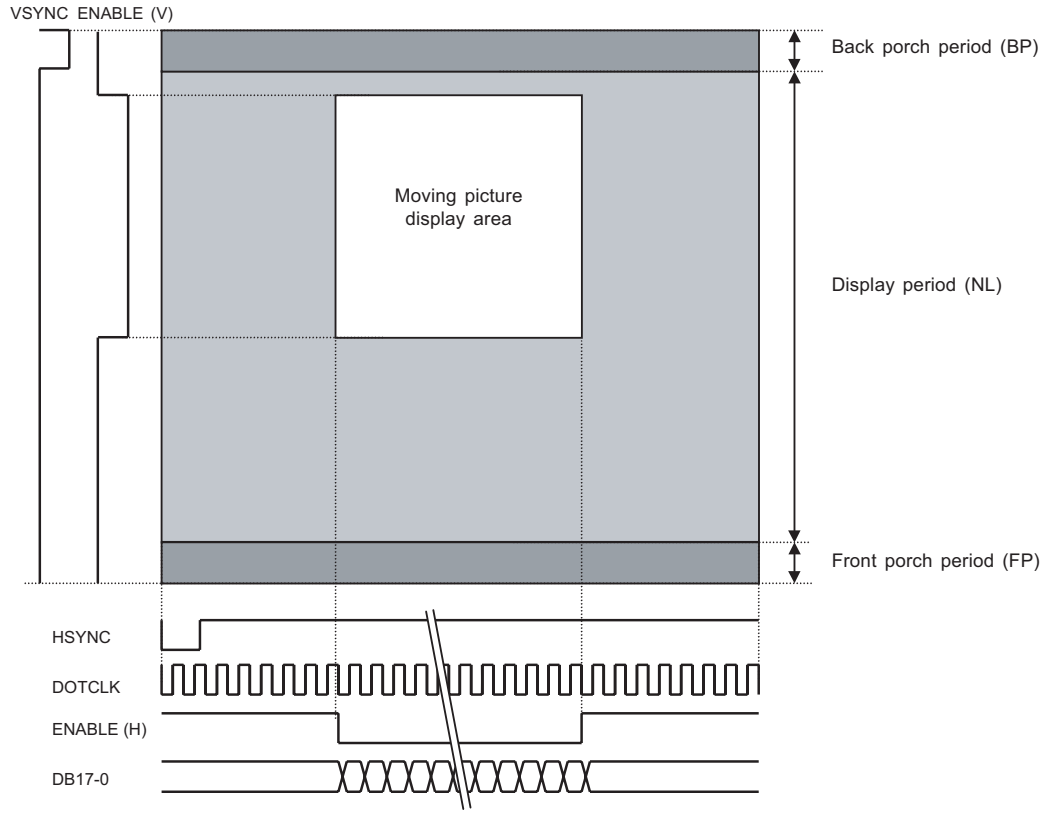
Table 92 RGB interface

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, DB11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting inhibited	-

Note: Using multiple interface at a time is prohibited.

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The data can be written only within the specified area with low power consumption by using window address function and high-speed write mode (HWM = 1). In RGB interface operation, front and back porch periods must be made before and after the display period.



VSYNC: Frame synchronization signal	Back porch period (BPP):	14H ≧ BP ≧ 2H
HSYNC: Line synchronization signal	Front porch period (FPP):	14H ≧ FP ≧ 2H
DOTCLK: Dot clock		FP + BP ≦ 16H
ENABLE: Data enable signal	Display period:	NL ≦ 432H
DB 17-0: RGB (6:6:6) display data	The number of lines for one frame:	FP + NL + BP

Notes: 1. The front porch period continues until next VSYNC input is detected.
2. Make sure to match the VSYNC, HSYNC, and DOTCLK frequencies to the resolution of liquid crystal panel.

Figure 66 Display Operation via RGB Interface

Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals can be changed by setting the DPL, EPL, HSPL, and VSPL bits, respectively for convenience of system configuration.

RGB Interface Timing

The timing relationship of signals in RGB interface operation is as follows.

16-/18-Bit RGB Interface Timing

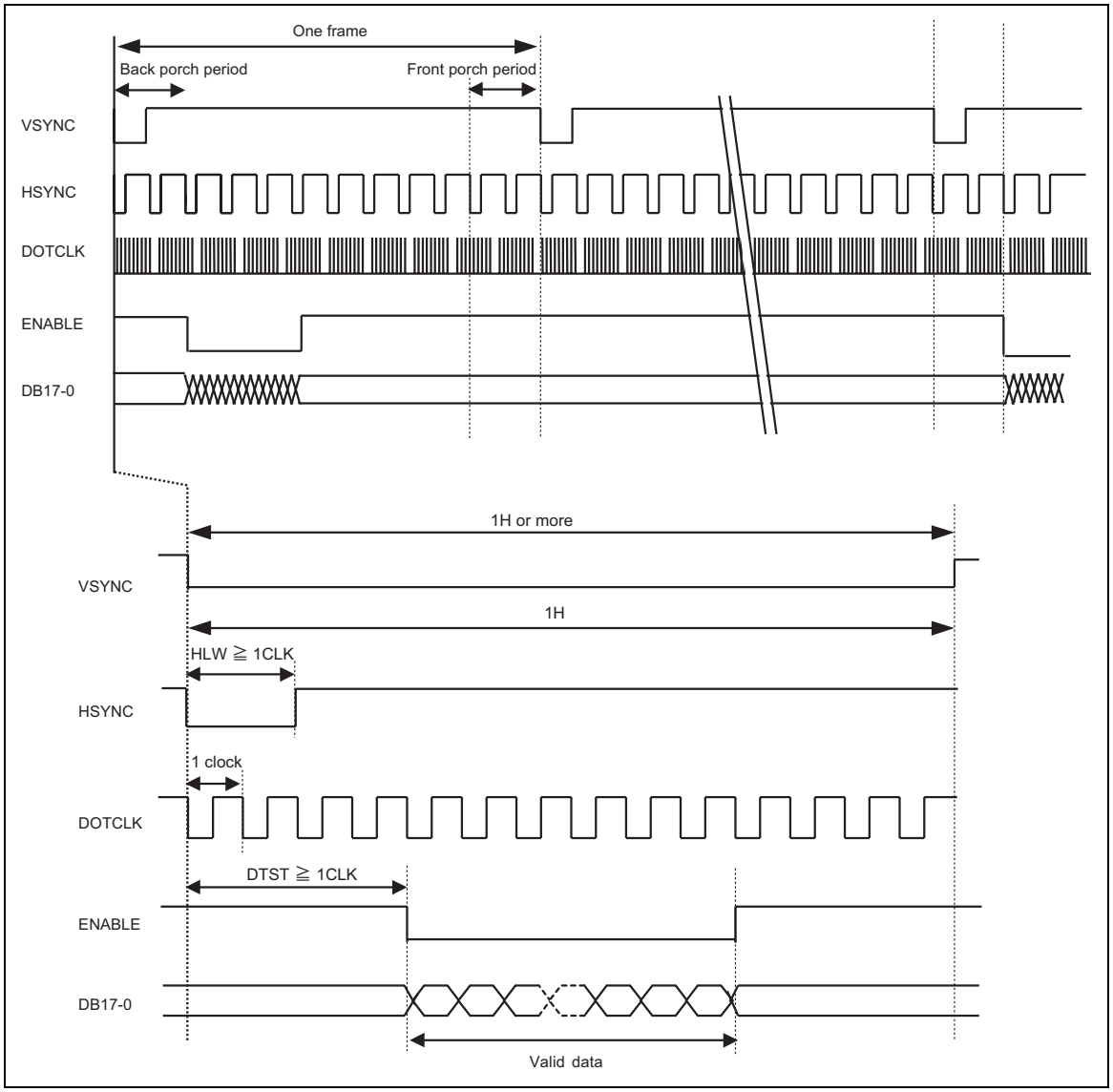


Figure 67

Notes: 1. VLW: VSYNC Low period
HLW: HSYNC Low period
DTST: data transfer setup time
2. Use high-speed write function (HWM = 1) when writing data via RGB interface.

6-Bit RGB Interface Timing

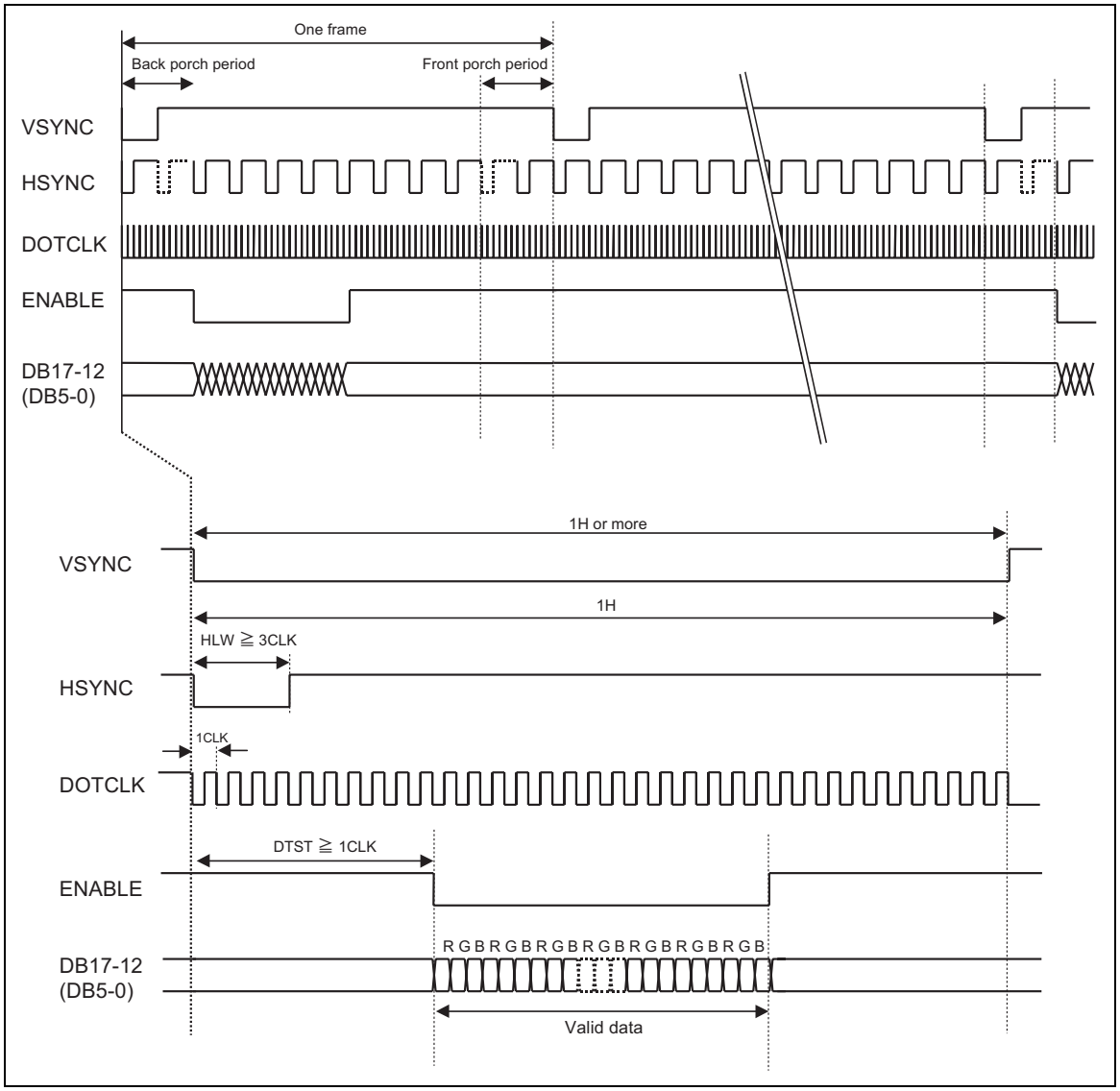


Figure 68

Notes: 1. VLW: VSYNC Low period
HLW: HSYNC Low period
DTST: Data transfer setup time

2. Use high-speed write function (HWM = 1) when writing data via RGB interface.
3. In 6-bit RGB interface operation, set the VSYNC, HSYNC, ENABLE, DOTCLK cycles so that one pixel is transferred in units of three DOTCLKs via DB17-12 (DB5-0).

Moving Picture Display via RGB Interface

The R61509 supports RGB interface for moving picture display and incorporates RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function enables transferring data only within the moving picture area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. It becomes possible to transfer only the data written over the moving picture area
4. By reducing data transfer, it can contribute to lowering the power consumption of the whole system
5. The data in still picture area (icons etc.) can be written over via system interface while displaying a moving picture via RGB interface

RAM access via system interface in RGB interface operation

The R61509 allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is "Low". When writing data to the RAM via system interface, set ENABLE "High" to stop writing data via RGB interface. Then set RM = "0" to enable RAM access via system interface. When reverting to the RGB interface operation, wait for the read/write bus cycle time. Then, set RM = "1" and the index register to R22h to start accessing RAM via RGB interface. If there is a conflict between RAM accesses via two interfaces, there is no guarantee that the data is written in the RAM.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

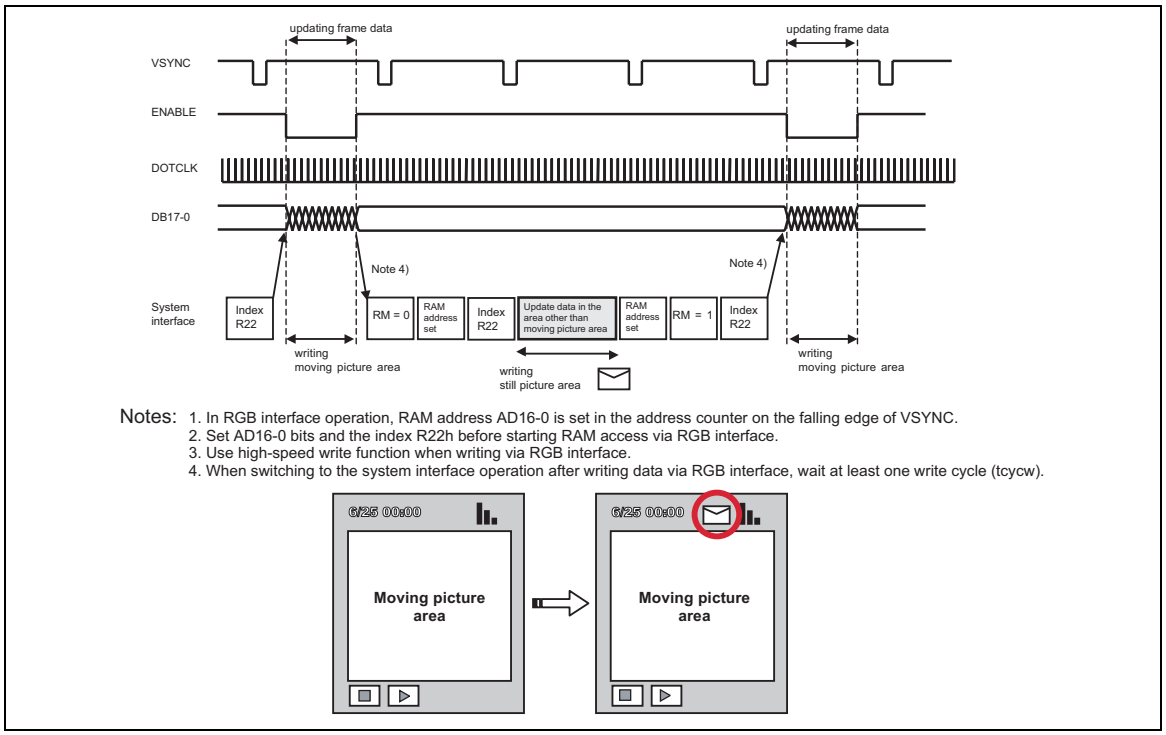


Figure 69 Updating the Still Picture Area while Displaying Moving Picture

6-Bit RGB interface

The 6-bit RGB interface is selected by setting RIM1-0 = 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit port while data enable signal (ENABLE) allows RAM access via RGB interface. Unused pins DB11-0 (DB17-6) must be fixed at either IOVCC1 or GND level.

Instruction bits can be transferred only via system interface.

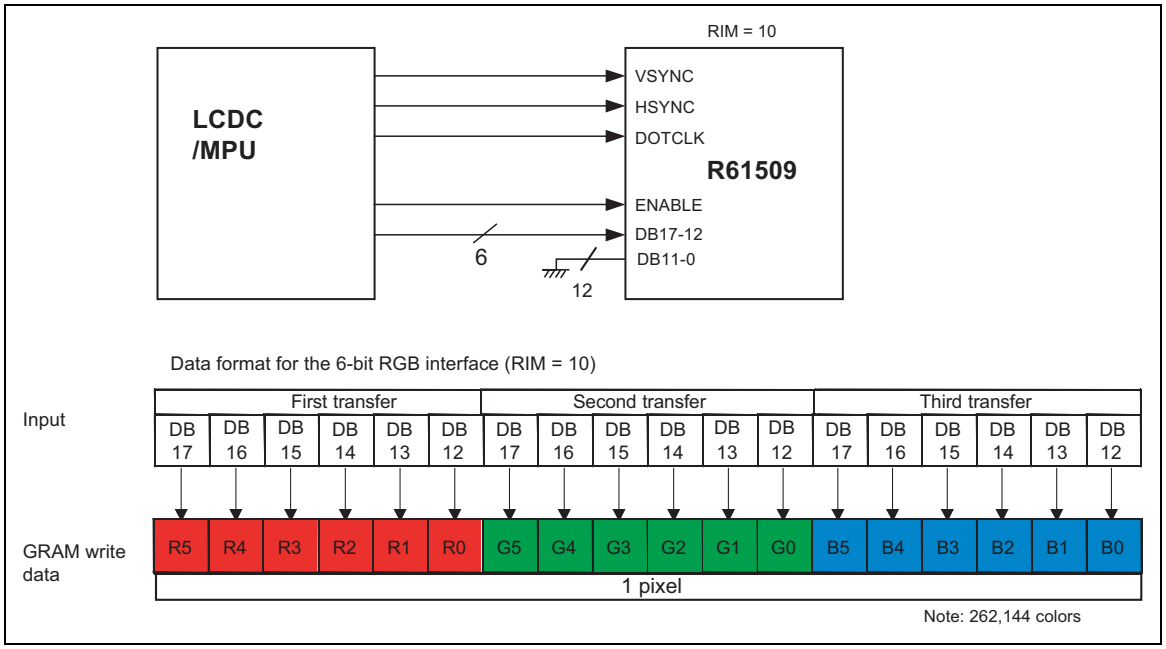


Figure 70 Example of 6-Bit RGB Interface and Data Format

Data Transfer Synchronization in 6-bit Bus Interface operation

The R61509 has the counters, which count the first, second, third 6 bit transfers via 6-bit RBG interface. The counters are reset on the falling edge of VSYNC so that the data transfer will start from the first 6 bits of 18-bit RGB data from the next frame period. Accordingly, the data transfer via 6-bit interface can restart in correct order from the next frame period even if a mismatch occurs in transferring 6-bit data. This function can minimizes the effect from data transfer mismatch and help the display system return to normal display operation when data is transferred consecutively in moving picture operation.

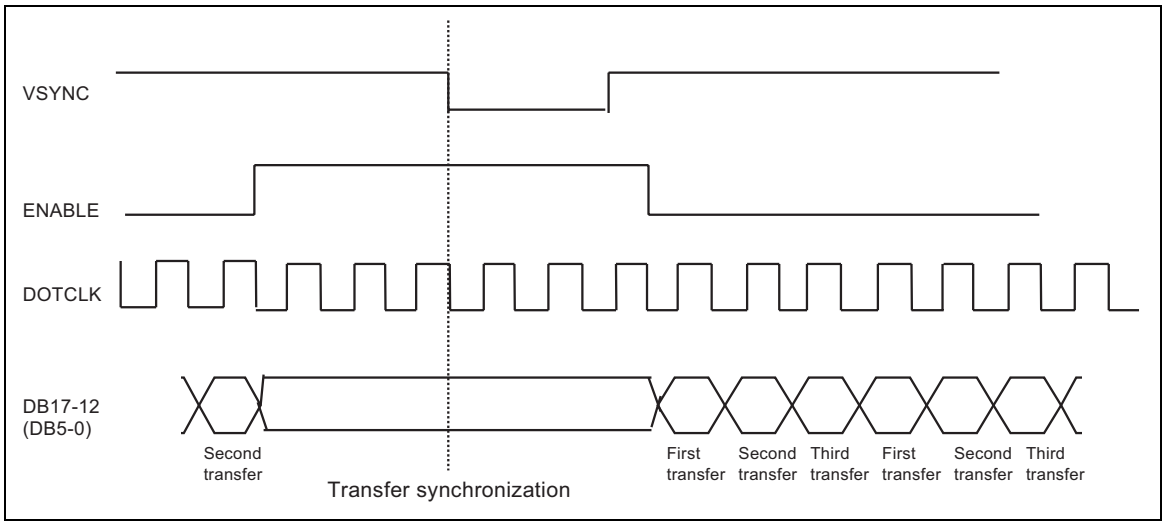


Figure 71 6-Bit Transfer Synchronization

16-Bit RGB Interface

The 16-bit RGB interface is selected by setting RIM1-0 = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit ports while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

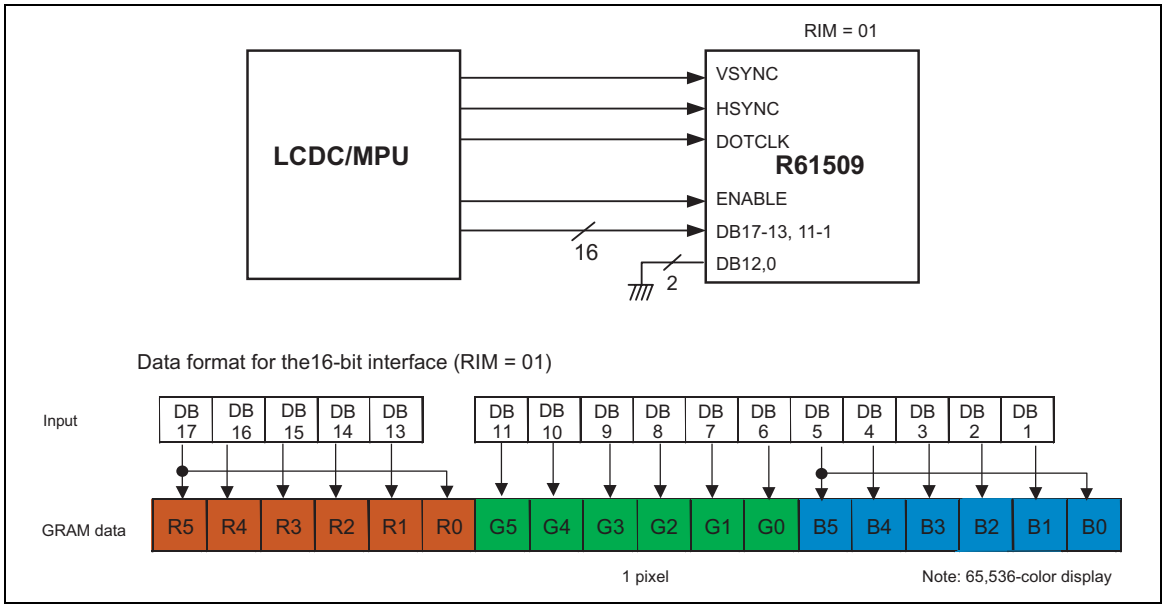


Figure 72 Example of 16-Bit RGB Interface and Data Format

18-bit RGB interface

The 18-bit RGB interface is selected by setting RIM1-0 = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit ports (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

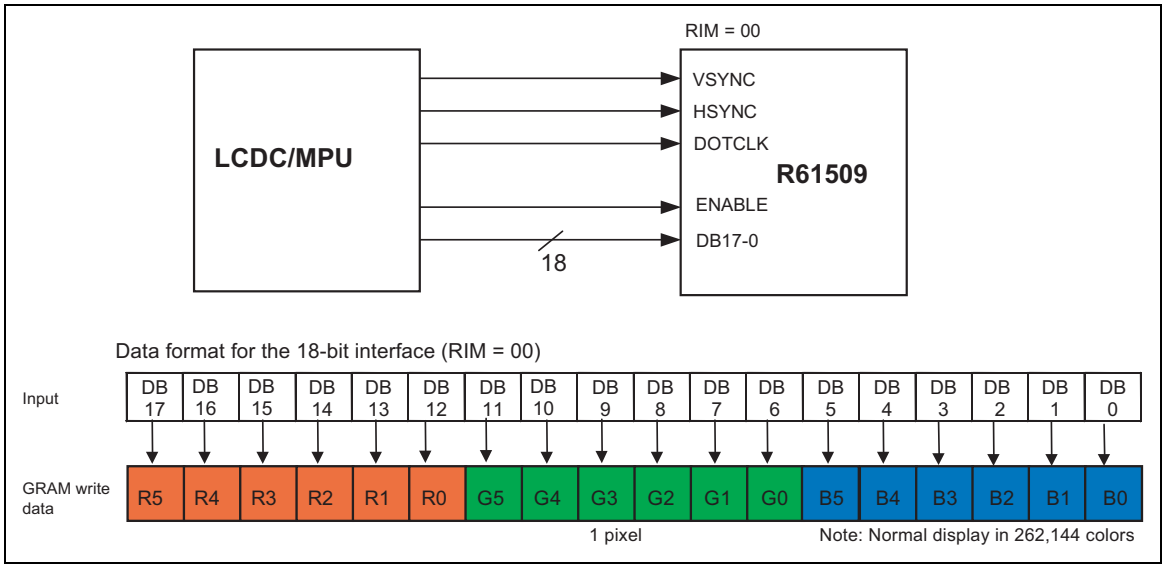


Figure 73 Example of 18-Bit RGB Interface and Data Format

Notes to RGB Interface Operation

1. The following functions are not available in RGB interface operation.

Table 93 Functions Not Available in RGB Interface operation

Function	RGB Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.
3. The reference clock to generate liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.
4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel data.
5. In 6-bit RGB interface operation, make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE signals so that the data transfer is completed in units of pixels.
6. When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.
7. In RGB interface operation, front porch period continues after the end of frame period until next VSYNC input is detected.
8. In RGB interface operation, use high-speed write function (HWM = 1) when writing data to the internal RAM.
9. In RGB interface operation, RAM address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

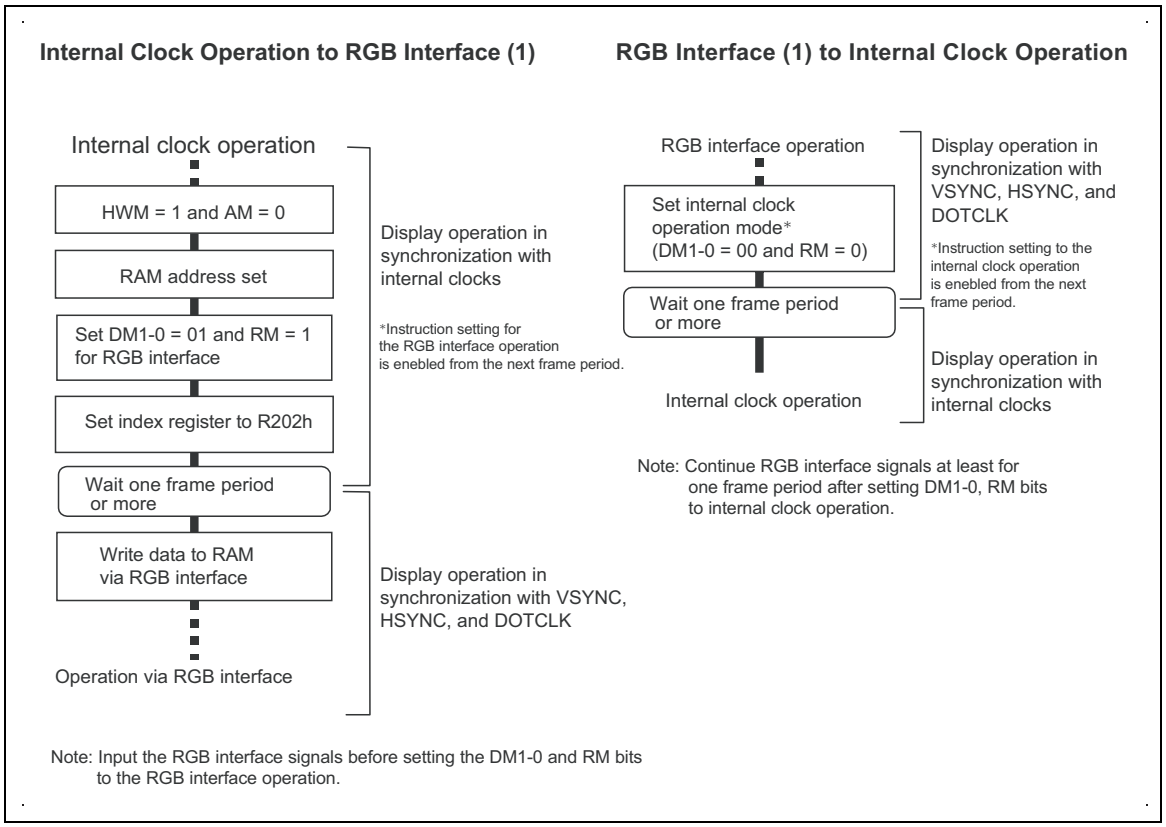


Figure 74 RGB and Internal Clock Operation Mode Switching Sequences

RAM Address and Display Position on the Panel

The R61509 has memory to store display data of 240RGB x 432 lines. The R61509 incorporates a circuit to control partial display, which allows switching driving method between full-screen display mode and partial display mode.

The R61509 makes display arrangement setting and panel driving position control setting separately and specifies RAM area for each image displayed on the panel.

The following is the sequence of setting full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image by setting PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

Normal display	BASEE = 1
Partial display 1/2	BASEE = 0, PTDE0/1 = 1

5. Changes BASEE, PTDE0/1 settings when turning on and off the full and partial displays 1/2.

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, set SS bit when writing RAM data.

Table 94

	Display ENABLE	Numbers of lines	RAM area
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h1AF)

Notes 1: The base image is displayed from the first line of the screen.

2: Make sure NL ≤ 432 (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h1AF, respectively.

Table 95

	Display ENABLE	Display position	RAM area
Partial image 1	PTDE0	PTDP0	(PTSA0, PTEA0)
Partial image 2	PTDE1	PTDP1	(PTSA1, PTEA1)

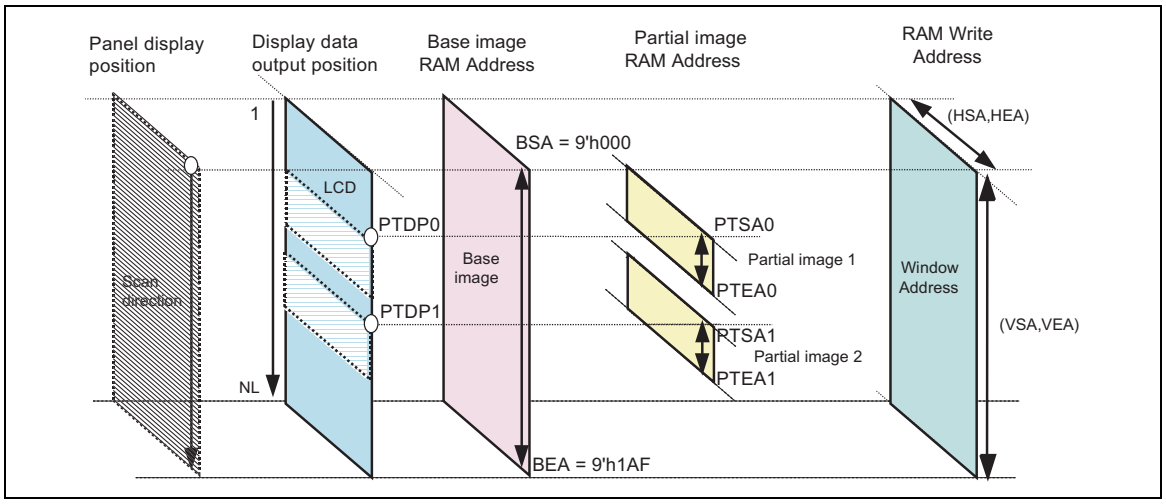


Figure 75 RAM Address, Display Position and Drive Position

Restrictions in Setting Display Control Instruction

There are restrictions in coordinates setting for display data, display position and partial display.

Screen setting

In setting the number of lines to drive the liquid crystal panel, make sure that the total number of lines is 432 lines or less (NL ≤ 432 lines).

Base image display

The base image is displayed from the first line of the screen: Base image display start position = 1st line

Partial image display

Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partial images do not overlap one another.

$$0 \le PTDP0 \le PTDP0 + (PTEA0 - PTSA0) < PTDP1 \le PTDP1 + (PTEA1 - PTSA1) \le NL$$

The following figure shows the relationship among the RAM address, display position, and the lines driven for the display.

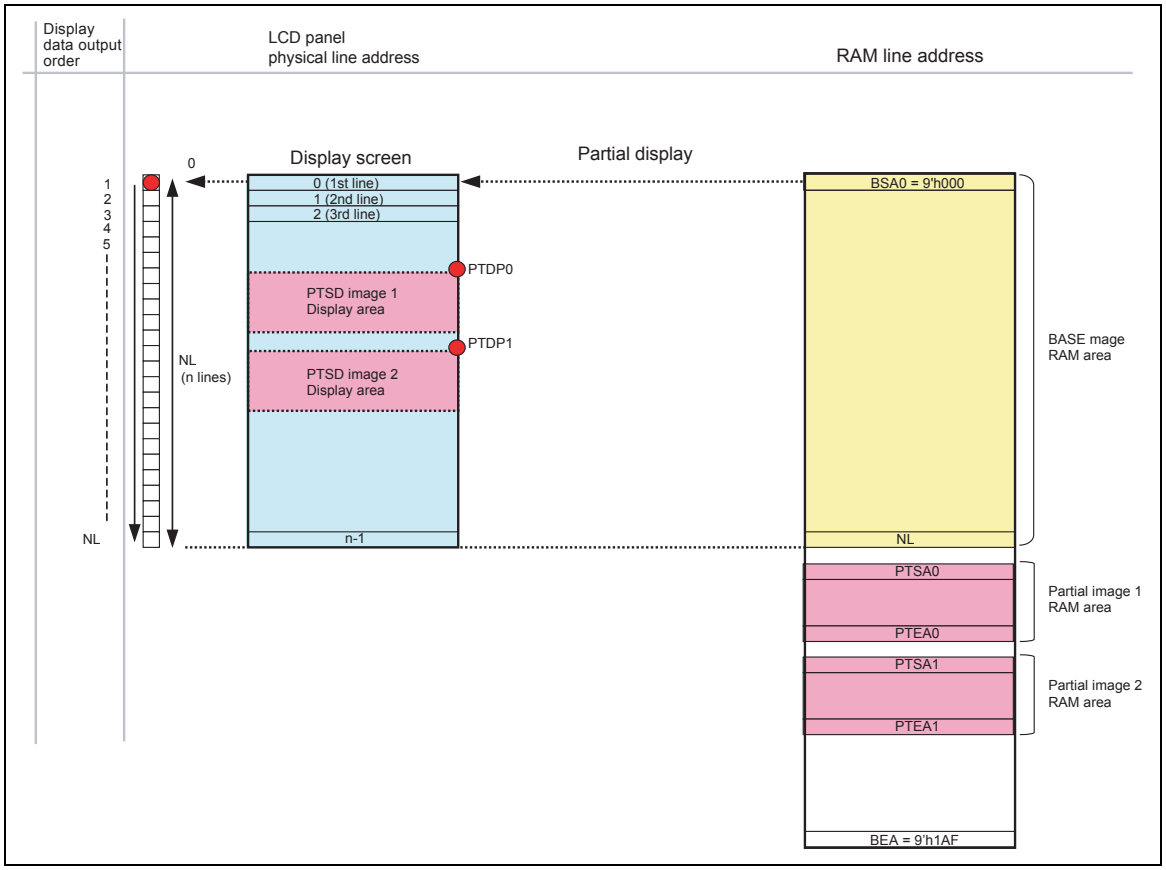


Figure 76 Display RAM Address and Panel Display Position

Note: This figure shows the relationship between RAM line address and the display position on the panel. In the R61509's internal operation, the data is written in the RAM area specified by the window address setting.

Instruction Setting Example

The followings are examples of settings for 240(RGB) x 432(lines) panel.

1. Full screen display (no partial display)

The following is an example of settings for full screen display.

Table 96

Base image display instruction	
BASEE	1
NL[5:0]	6'h35

PTDE0	0
PTDE1	0

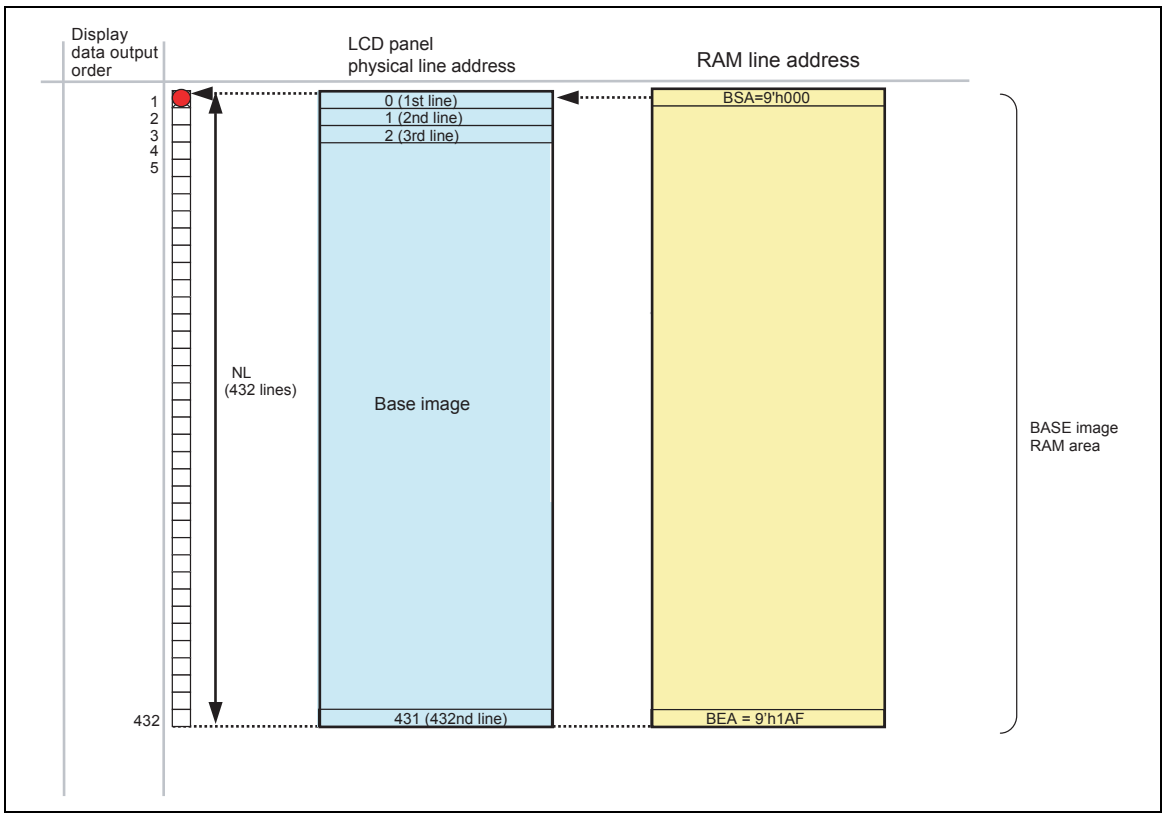


Figure 77 Full Screen Display (no Partial)

2. Partial only

The following is an example of settings for displaying partial image 1 only and turning off the base image. The partial image 1 is displayed at the position specified by PTDP0 bit.

Table 97

Base image display instruction	
BASEE	0
NL[5:0]	6'h35

partial image 1 display instruction	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080

partial image 2 display instruction	
PTDE1	0
PTSA1[8:0]	9'h000
PTEA1[8:0]	9'h000
PTDP1[8:0]	9'h000

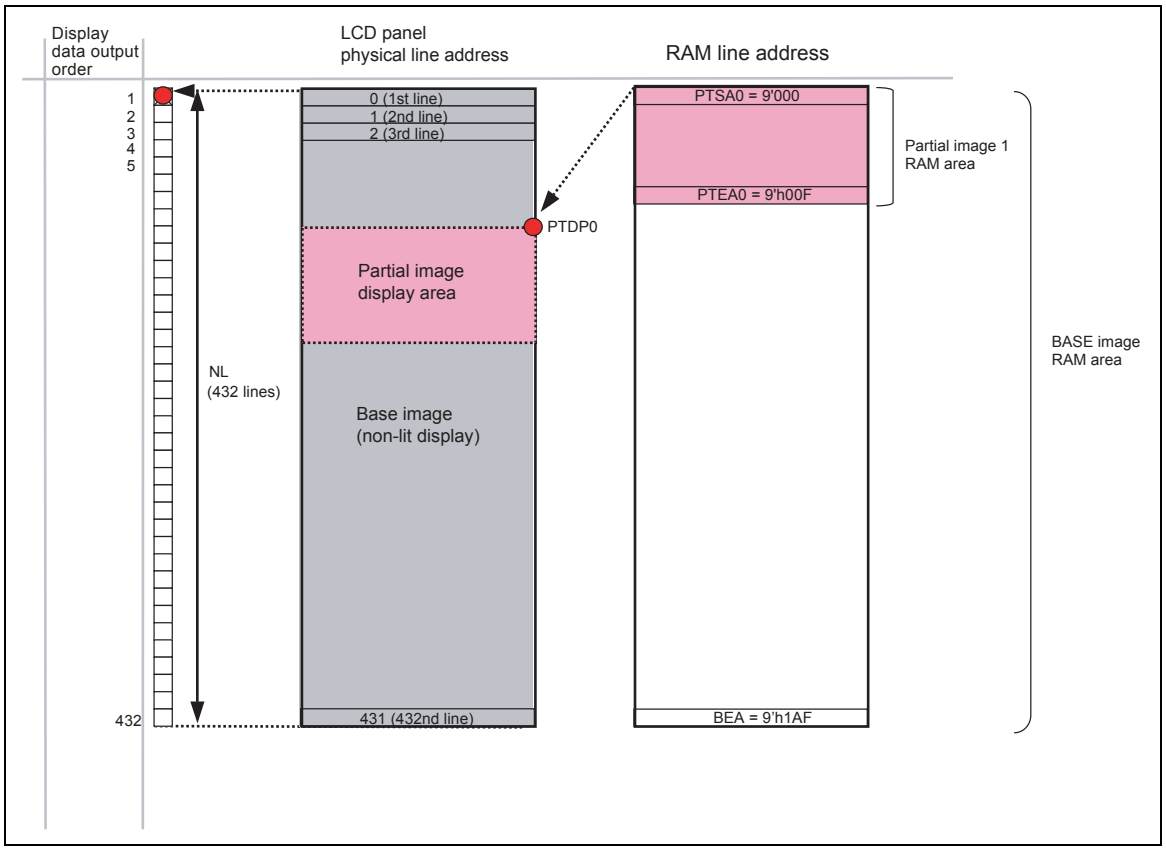


Figure 78 Partial Display

Outline Sharpening Function

The R61509 supports outline sharpening function. Image data, outline sharpened, can be written onto the RAM by setting image processing parameters, AVST, ADST, DTHU and DTHL, and EGMODE=1 and then transfer original data to designated window address.

*Note: Dummy write must be inserted every frame of RAM write operation. (See the following waveforms.)

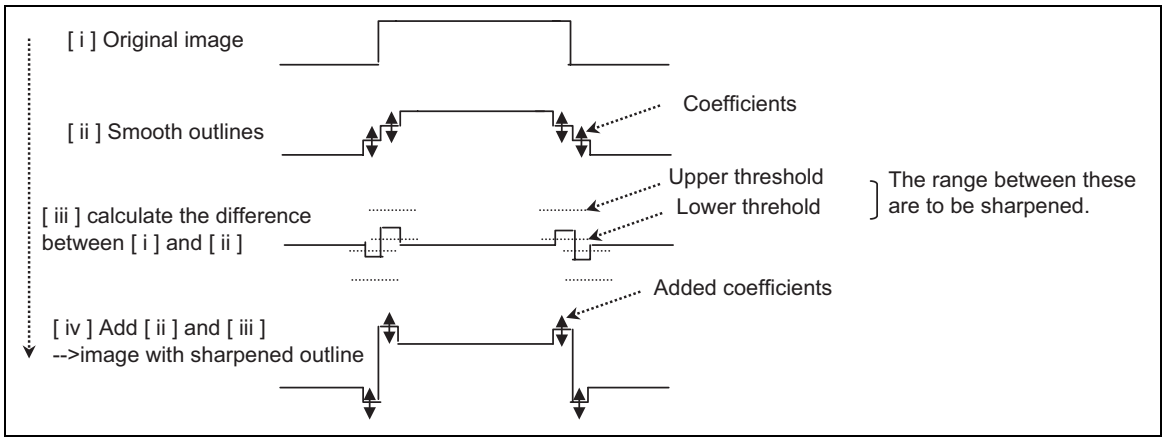
Because this function operates calculating data of pixels, images with sharp outlines can be realized regardless of moving or still images.

The characteristics of algorithm used in this function may not fit some types of data to realize desirable result. Please confirm images after outline sharpening operation.

How to set outline sharpening instruction

In the R61509 AVST, ADST, DTHU and DTHL bits set parameters that adjust image data.

The following figure shows how the parameters and each stages of operational sequence interact.



Outline Sharpening Instruction: R006h

■Outline sharpening mode setting

EGMODE	Outline sharpening mode
1'h0	OFF
1'h1	ON

■ **Coefficients to smooth edges between neighboring pixels**

AVST[2:0]	Coefficients
3'h00	0.125(=1/8)
3'h01	0.250(=2/8)
3'h02	0.375(=3/8)
3'h03	0.500(=4/8)
3'h04	0.625(=5/8)
3'h05	0.750(=6/8)
3'h06	0.875(=7/8)
3'h07	1.000(=8/8)

■ **Added coefficients**

ADST[2:0]	Added coefficients
3'h00	0.0 (Off)
3'h01	0.5(=1/2)
3'h02	1.0(=2/2)
3'h03	1.5(=3/2)
3'h04	2.0(=4/2)
3'h05	2.5(=5/2)
3'h06	3.0(=6/2)
3'h07	3.5(=7/2)

■ **Higher threshold**

DTHU[1:0]	High threshold of the brightness band
2'h00	15
2'h01	31
2'h02	47
2'h03	63

■ **Lower threshold**

DTHL[1:0]	Lower threshold of the brightness band
2'h00	0
2'h01	Setting Disabled
2'h02	1
2'h03	2

Restriction to outline sharpening function

1. Outline sharpening instruction should be set before writing data to RAM.
2. RAM address update direction setting is restricted to AM=0 and I/D=2'b11.
3. When writing data to RAM, dummy write must be done 5 times consecutively right after transferring data of one frame that is set by window address setting. (See following waveforms.)
4. One pixel at the end of original data will not be sharpened.

Outline sharpening function RAM write-in sequence

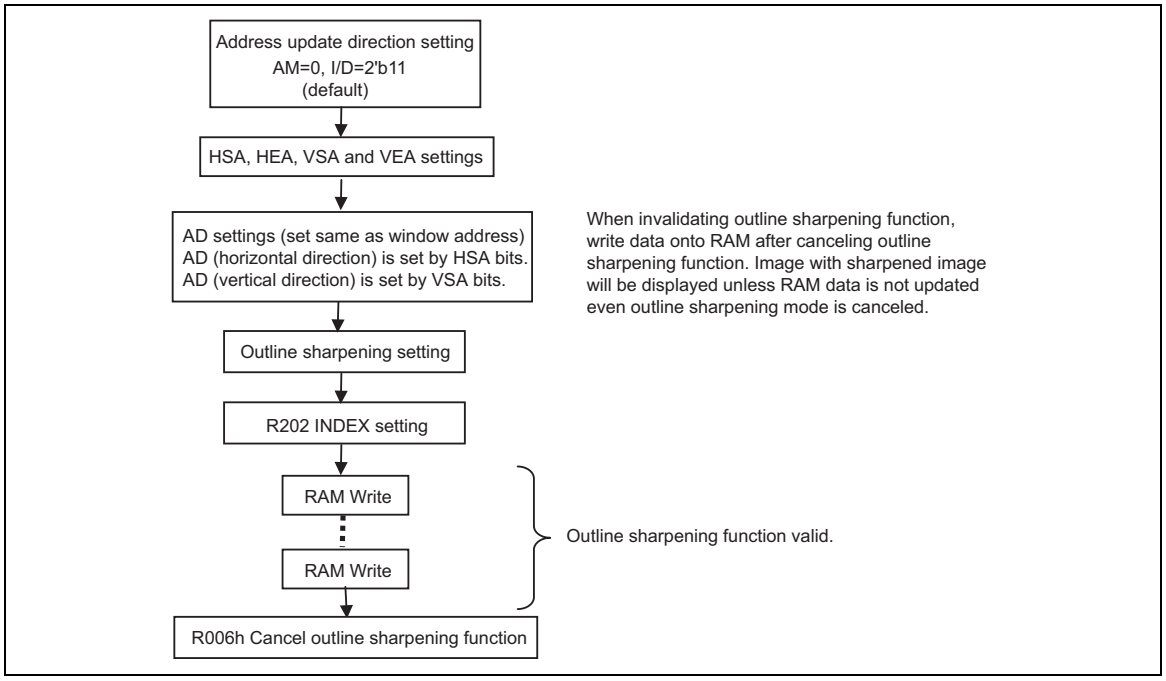


Figure 79

■Data transferring when 80-system VSYNC interface is selected

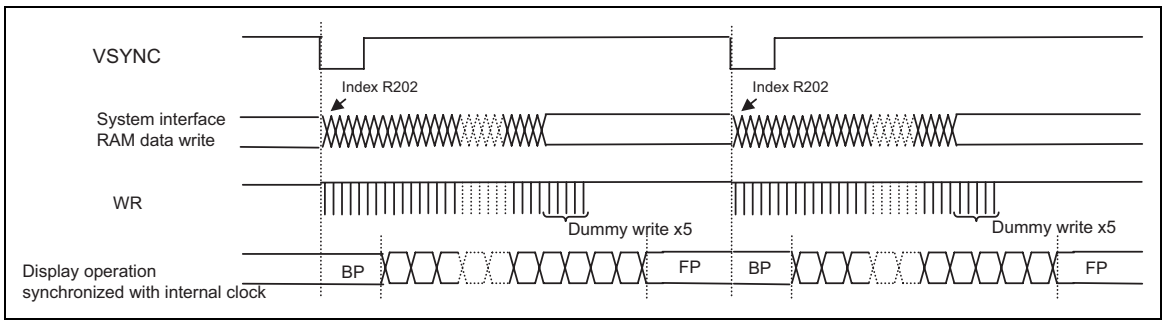


Figure 80

■Data transfer when 80-system FMARK interface is selected

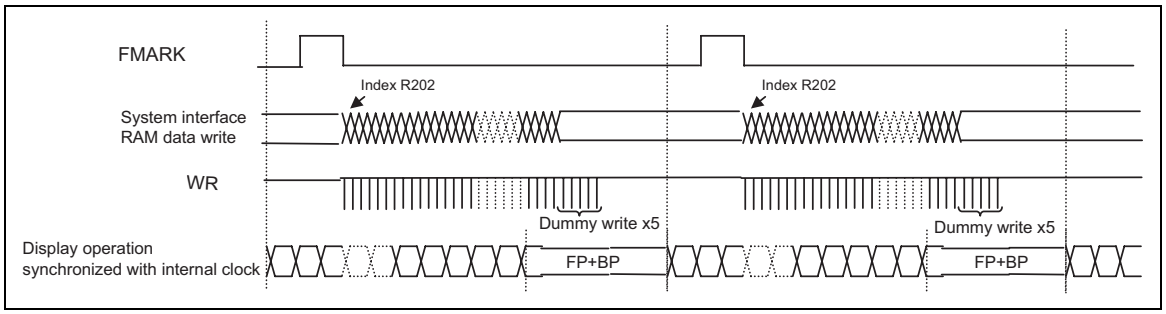


Figure 81

■2-frame data transfer when MDDI-VSYNC interface is selected

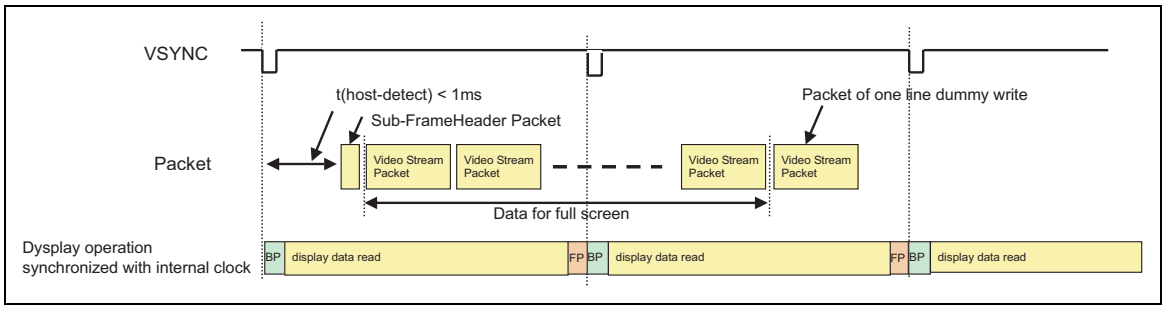


Figure 82

■2-frame data transfer when MDDI-FMARK interface is selected

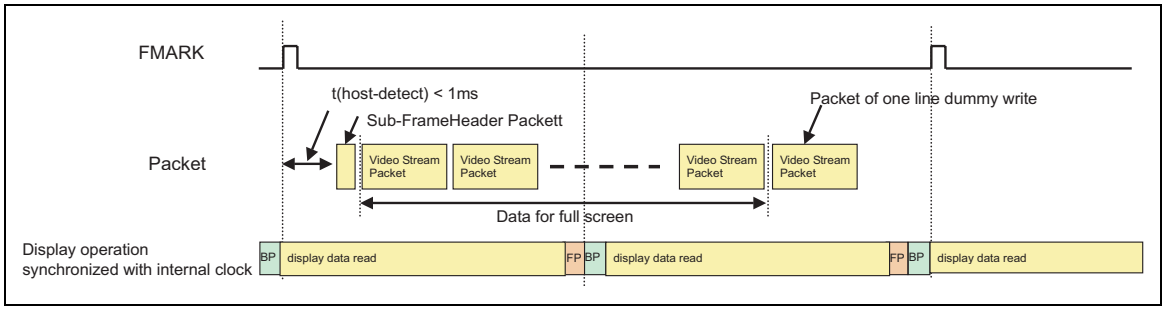


Figure 83

■Data transfer when RGB interface is selected

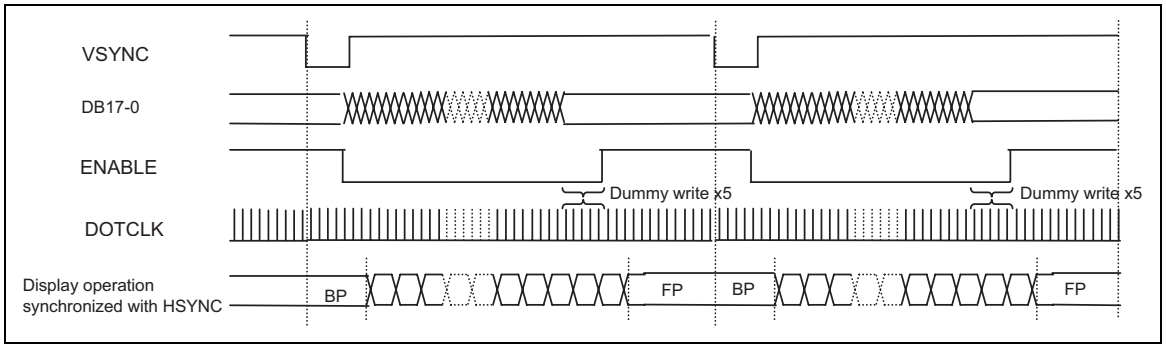


Figure 84

High-Speed RAM Write Function

The R61509 supports high-speed RAM write function to write data to each line of window address area at a time. This function makes the R61509 available with the applications, which require high-speed, low-power-consumption data write operation such as color moving picture display.

When enabling high-speed RAM write function (HWM = "1"), the data is first stored in the internal register of the R61509 in order to rewrite the RAM data in each horizontal line of the window address area at a time. Also, when transferring the data from the internal register to the internal RAM, the data written in the next line of the window address area can be transferred to the internal register of the R61509. The high-speed write function minimizes the number of RAM access in write operation and enables high-speed consecutive RAM write operation required for moving picture display with low power consumption.

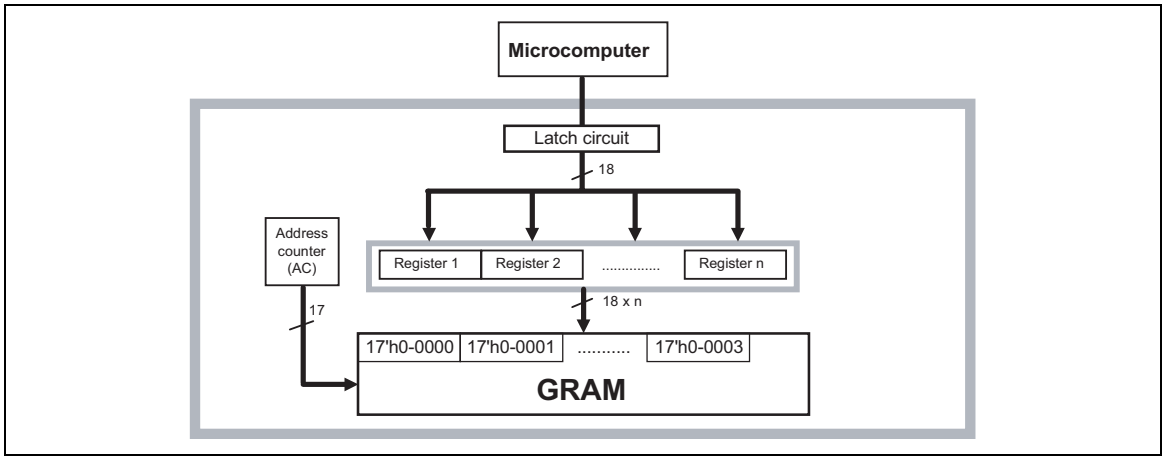


Figure 85 High-Speed Consecutive RAM Write Operation

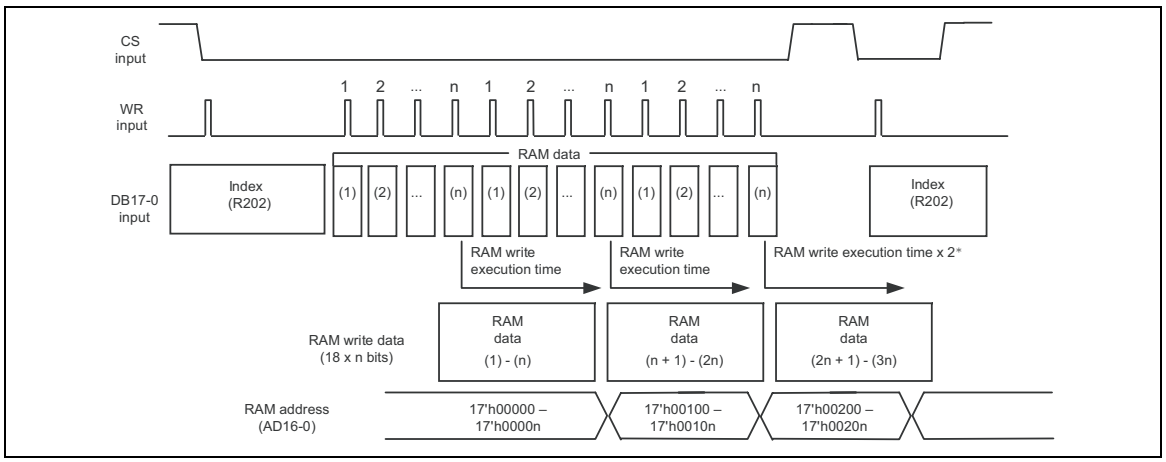


Figure 86 Example of High-Speed RAM Write Operation (HWM = 1)

Note: When switching from high-speed RAM write operation to index write operation, wait at least for two normal RAM write bus cycle periods (2 x t_{cycw}) before executing a next instruction.

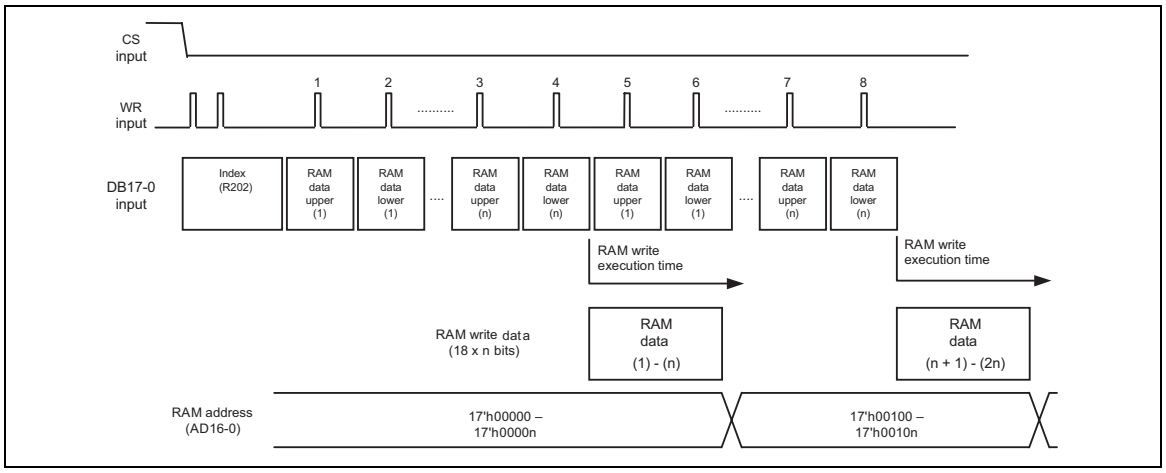


Figure 87 Example of High-Speed RAM Write Operation via 9-Bit Interface

Note: In high-speed RAM write operation, the R61509 writes data in units of n words. When using 9-bit interface, the R61509 performs write operation 2 x n times in the internal register before writing the data in each line of the window address area.

Notes to High-Speed RAM Write Function

1. In high-speed RAM write mode, the R61509 performs write operation to the internal RAM in units of lines. If the data inputted to the internal write register is not enough to rewrite the data in the horizontal line of the window address area, the data is not written correctly in that line address.

2. If the IR is set to 22h when HWM = "1", the R61509 always performs RAM write operation. With this setting, the R61509 does not perform RAM read operation. Make sure to set HWM = 0, when performing RAM read operation.

3. The high-speed RAM write function cannot be used when writing data in normal RAM write function mode. When switching form one write mode to the other, change modes first and set AD16-0 (RAM address set) before starting write operation.

Table 98 RAM Write Operation

	Normal RAM Write (HWM = 0)	High-speed RAM Write (HWM = 1)
BGR function	Available	Available
RAM address set	In units of words	In units of words
RAM read	In units of words	Not available
RAM write	In units of words	In units of lines
Window address	In units of words (minimum window address area: 1 word x 1 line)	In units of words (minimum window address area: 8 words x 1 line)
External display interface	Available	Available
AM	AM = 1/0	AM = 0

High-Speed RAM Data Write in a Window Address Area

The R61509 can perform consecutive high-speed data rewrite operation within a rectangular area (minimum: 8 words x 1 line) made in the internal RAM with the following settings.

When writing data to the internal RAM using high-speed RAM write function, make sure each line of the window address area is overwritten at a time. If the data buffered in the internal register of the R61509 is not enough to overwrite the horizontal line in the window address area, the data is not written correctly in that line.

The following is an example of writing data in the window address area using high-speed write function when a window address area is made by setting HSA = 8'h12, HEA = 8'hA7, VSA = 9'h020, and VEA = 9'h05B.

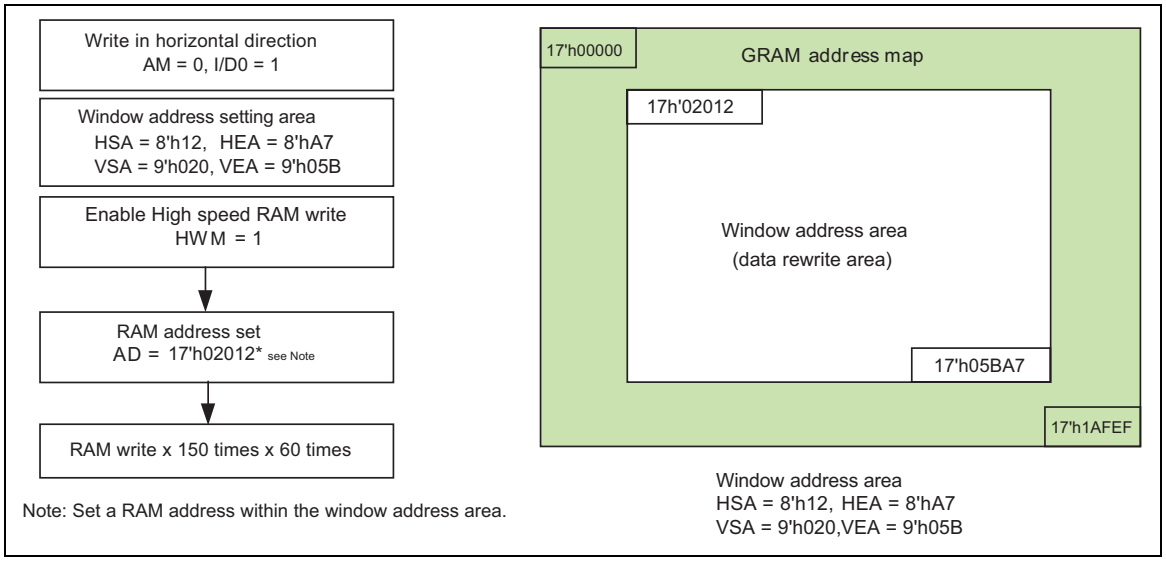


Figure 88 High-Speed RAM Write Operation in the Window Address Area

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is described by the horizontal address register (start: HSA7-0, end: HEA7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the R61509 to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area setting range]
(Horizontal direction) 8'h00 ≤ HSA ≤ HEA ≤ 8'hEF
(Vertical direction) 9'h000 ≤ VSA ≤ VEA ≤ 9'h1AF

[RAM Address setting range]
(RAM address) HSA ≤ AD7-0 ≤ HEA
VSA ≤ AD16-8 ≤ VEA

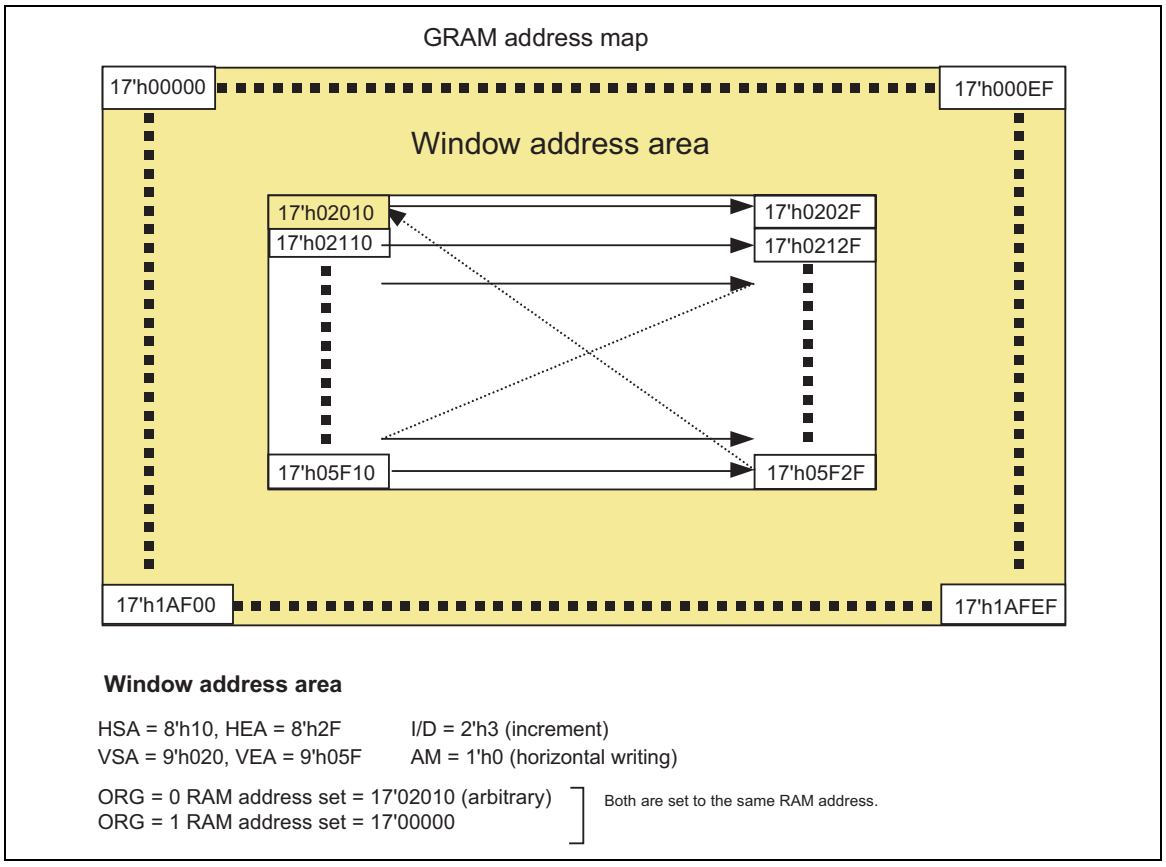
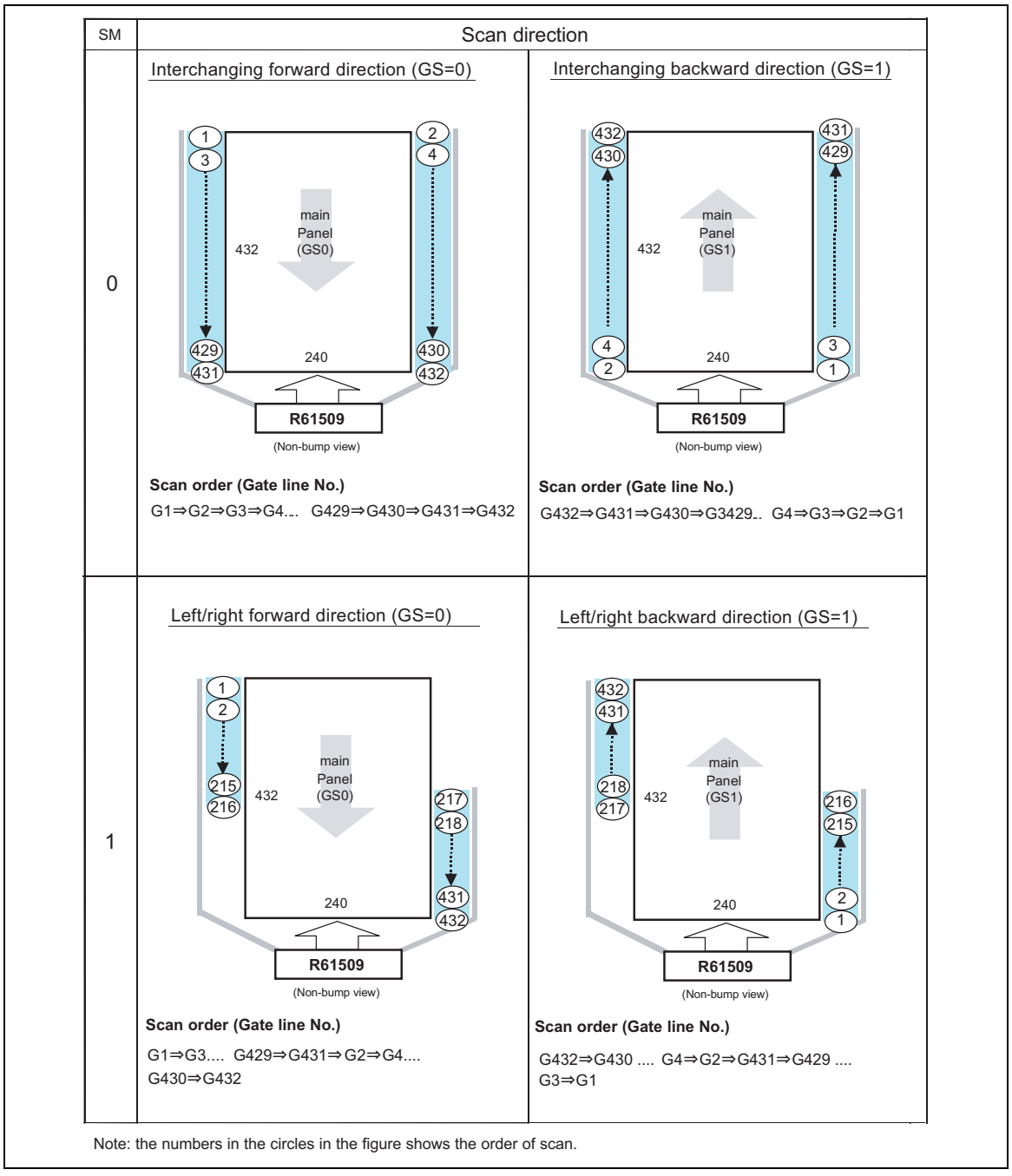


Figure 89 Automatic Address Update within a Window Address Area

Scan Mode Setting

The R61509 can set the gate pin assignment and the scan direction in the following 4 different ways by setting SM and GS bits to realize various connections between the R61509 and the LCD panel.



Note: the numbers in the circles in the figure shows the order of scan.

Figure 90

8-Color Display Mode

The R61509 has a function to display in eight colors. In this display mode, only V0 and V31 are used and power supplies to other grayscales (V1 to V30) are turned off to reduce power consumption.

In 8-color display mode, the γ-adjustment registers P0KP0-P0KP5, P0KN0-P0KN5, P0RP0, P0RP1, P0RN0, P0RN1, P0FP0-P0FP3, and P0FN0-P0FN3, are disabled and the power supplies to V1 to V30 are halted. The R61509 does not require GRAM data rewrite for 8-color display by writing the MSB to the rest in each dot data to display in 8 colors.

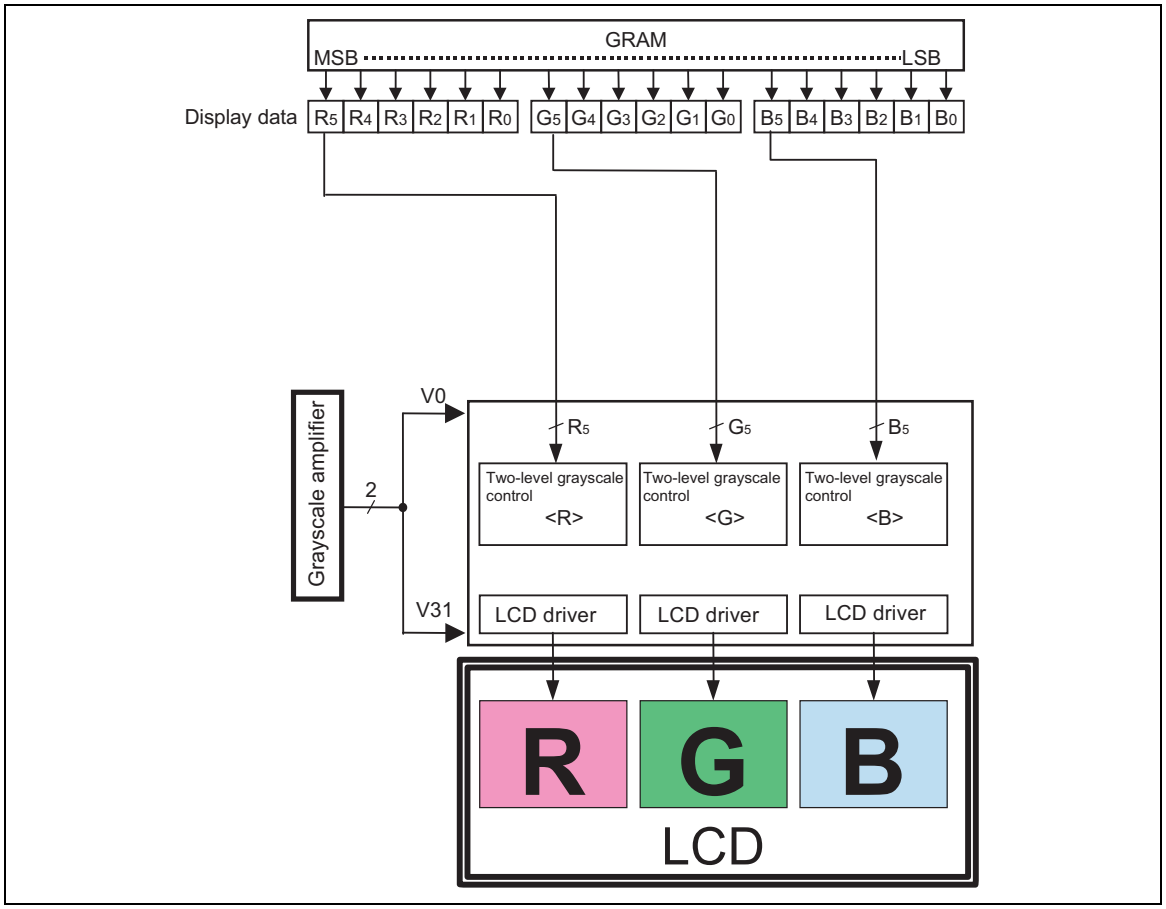


Figure 91 8-Color Display Mode

N-Line Inversion AC Drive

In addition to frame-inversion liquid crystal alternating current drive, the R61509 supports N-line inversion alternating current drive. The polarity is inverted every 1, 2, 3, or 4 line(s) according to register setting. This N-line inversion may be effective in solving display quality issue. Set N (NW bit + 1) checking the image quality on the panel. Note that when N is smaller, alternating frequency at the liquid crystal is higher, causing more current charged or discharged at TFT cells.

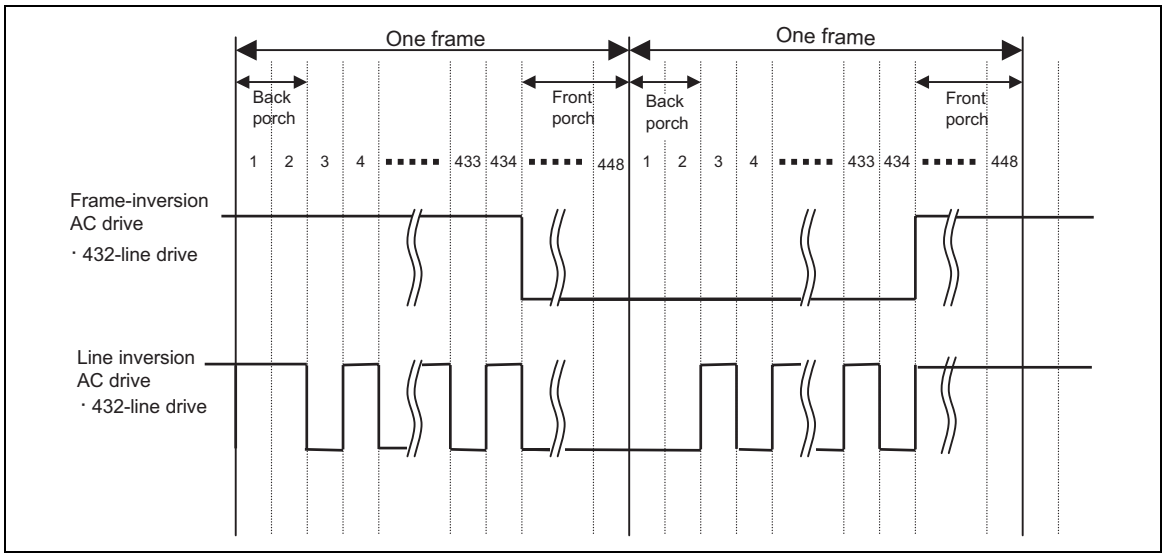


Figure 92 Example of Alternating Signals for N-Line Inversion

Note: During blank period (back and front porch periods), alternation halts to start again at the first line of next display period.

Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different LCD driving methods. In case of frame-inversion AC drive, the polarity is inverted as the R61509 draws one frame, which is followed by a blank period lasting for (BP+FP) periods. In line inversion AC drive, polarity is inverted as the R61509 draws one line, and a blank period lasting for (BP+FP) periods is inserted when one frame is drawn.

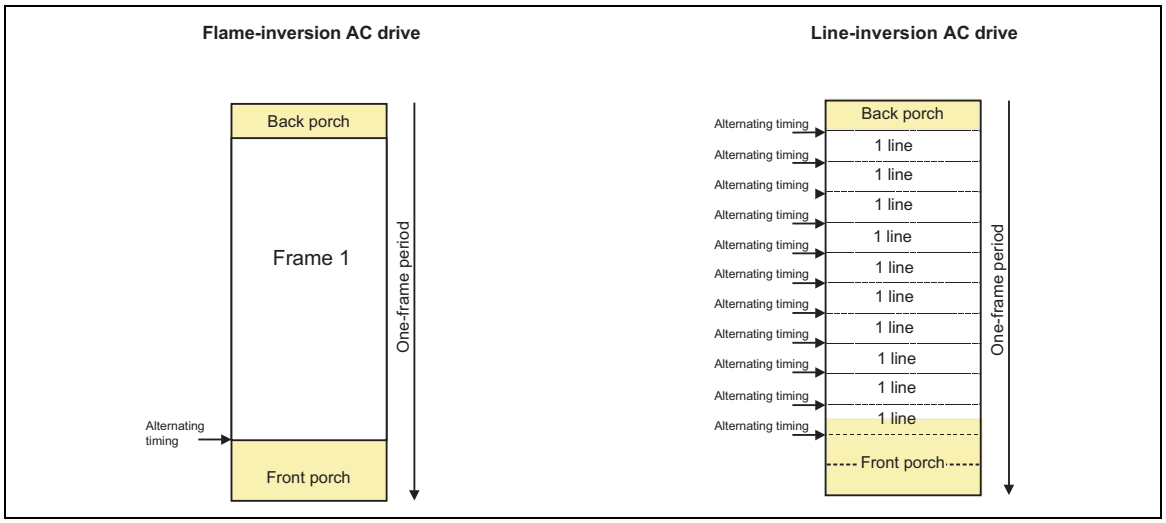


Figure 93 Alternating Timing

Frame-Frequency Adjustment Function

The R61509 supports a function to adjust frame frequency. The frame frequency for driving liquid crystal can be adjusted by setting the DIV, RTN bits without changing the oscillation frequency.

By changing the DIV and RTN settings, the R61509 can operate at high frame frequency when displaying a moving picture, which requires the R61509 to rewrite data in high speed, and it can operate at low frame frequency when displaying a still picture.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The following equation represent the relationship between liquid crystal drive duty and frame frequency. The frame frequency can be changed by setting the 1H period adjustment bit (RTN) and the operation clock frequency division ratio setting bit (DIV).

Equation for calculating frame frequency

$$FrameFrequency = \frac{fosc}{NumberofClocks/line \times DivisionRatio \times (Line + FP + BP)}[Hz]$$

fosc: RC oscillation frequency
Number of clocks per line: RTNI bit
Division ratio: DIVI bit
Line: number of lines to drive the LCD panel (NL bit)
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when maximum frame frequency = 60 Hz

fosc: 678 kHz
Number of lines: 432 lines
1H period: 25 clock cycles (RTNI [4:0] = "11001")
Division ratio of operating clock: 1/1
Front porch: 2 lines
Back porch: 14 lines

$$f_{FLM} = 678\ (kHz) / 25\ (clocks) \times 1/1 \times (432+2+14)\ (lines) \fallingdotseq 60.5\ (Hz)$$

Under the above conditions, the frame frequency can be changed according to the table shown below.

Table 99 Frame Frequency Setting (NL = 432 lines, BP = 14 lines, FP = 2 lines, fosc = 678 kHz)

RTNI[4:0]	DIVI = 2'h0	DIVI = 2'h1
5'h00 - 5'h0F	-	-
5'h10	95 Hz	47 Hz
5'h11	89 Hz	45 Hz
5'h12	84 Hz	42 Hz
5'h13	80 Hz	40 Hz
5'h14	76 Hz	38 Hz
5'h15	72 Hz	36 Hz
5'h16	69 Hz	34 Hz
5'h17	66 Hz	33 Hz
5'h18	63 Hz	32 Hz
5'h19	61 Hz	30 Hz
5'h1A	58 Hz	29 Hz
5'h1B	56 Hz	28 Hz
5'h1C	54 Hz	27 Hz
5'h1D	52 Hz	26 Hz
5'h1E	50 Hz	25 Hz
5'h1F	49 Hz	24 Hz

Partial Display Function

The partial display function allows the R61509 to drive lines selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven at non-lit display level to reduce power consumption.

The power efficiency can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

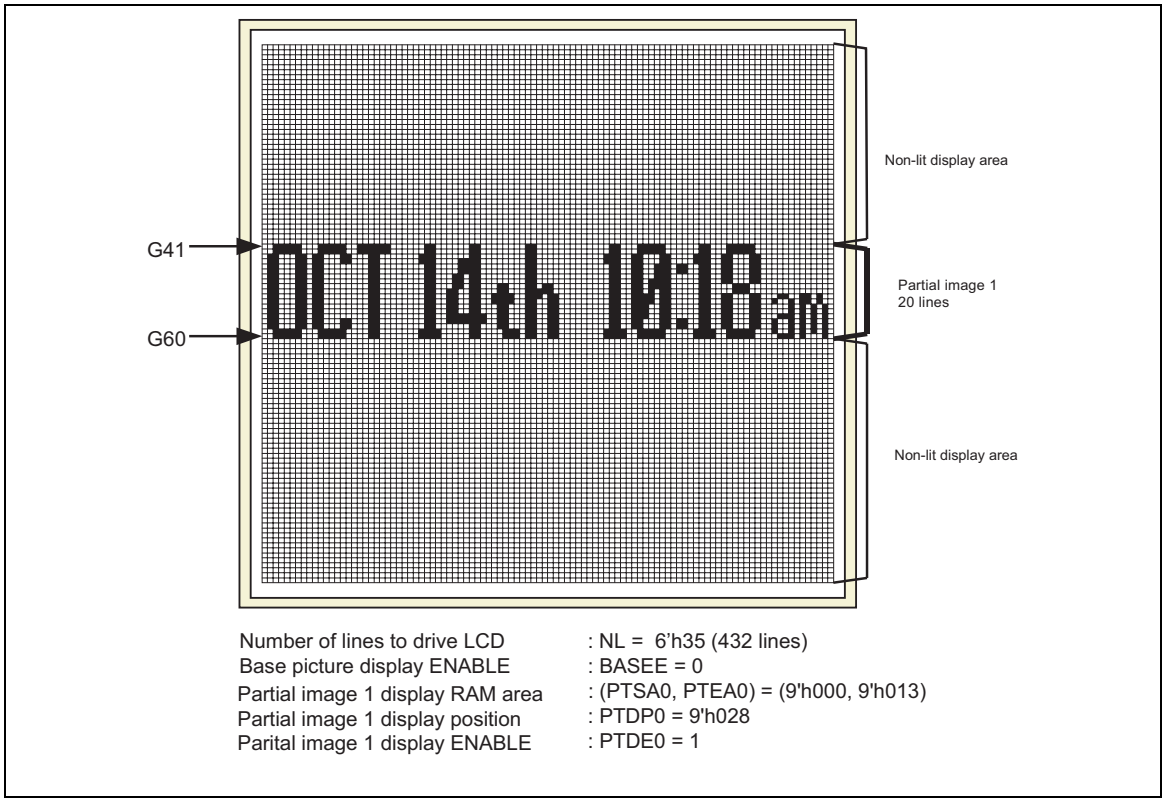


Figure 94 Partial Display

Note: See the RAM Address and Display Position on the Panel for details on the relationship between the display positions of partial images and respective RAM area setting.

Liquid Crystal Panel Interface Timing

The relationships between RGB interface signals and liquid crystal panel control signals in internal operation and RGB interface operations are as follows.

Internal Clock Operation

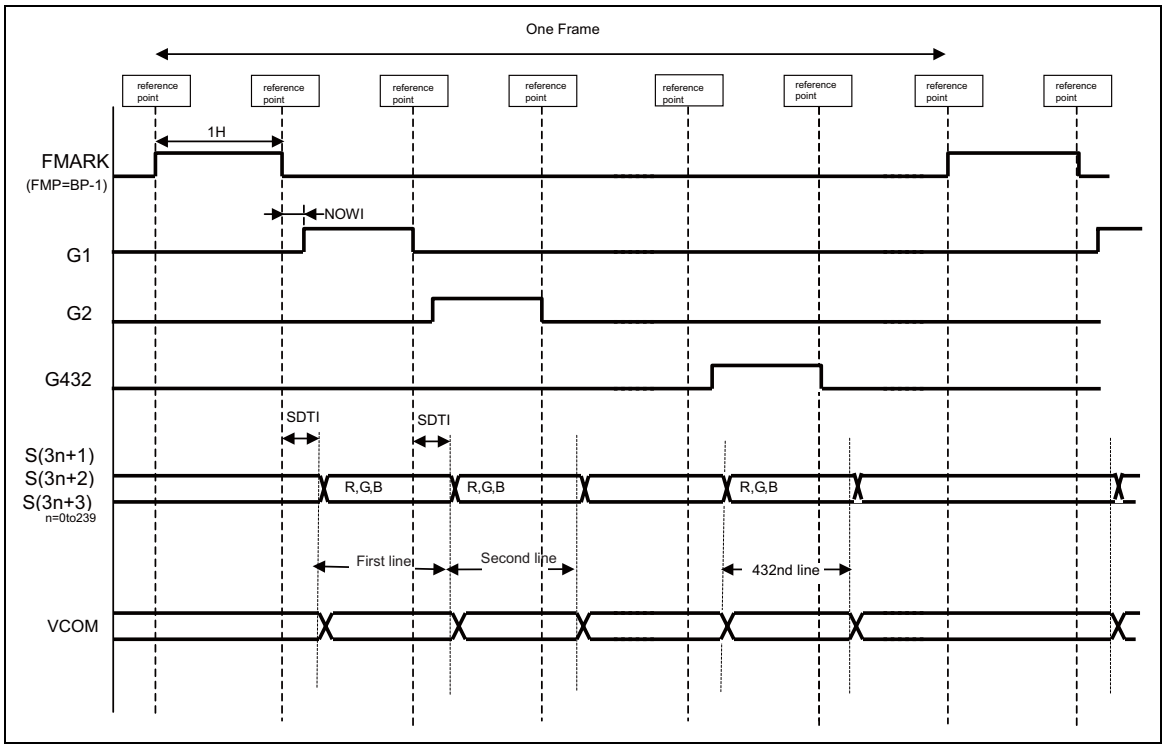


Figure 95

RGB Interface Operation

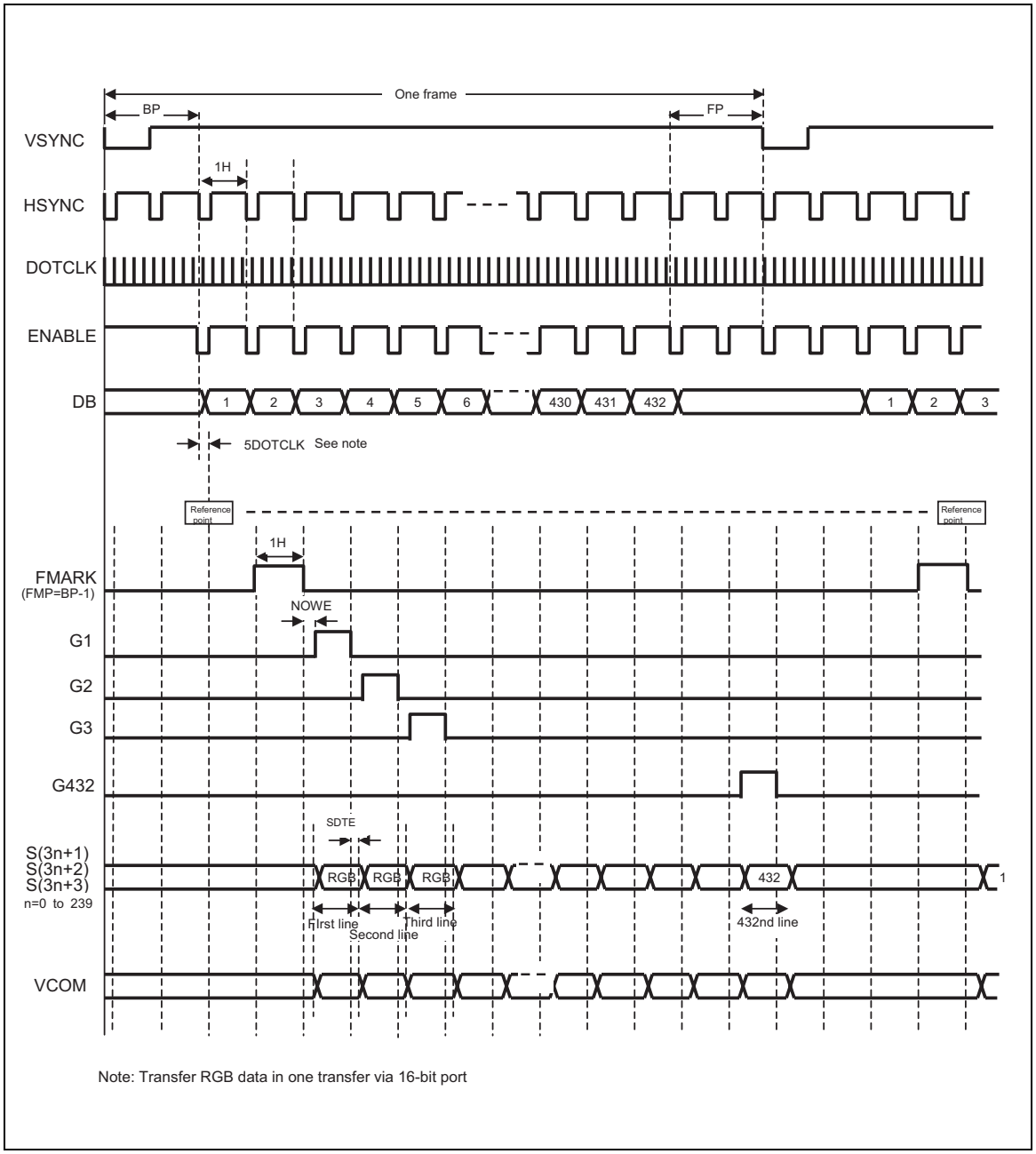


Figure 96

γ Correction Function

The R61509 supports γ-correction function to display in 262,144 colors simultaneously using gradient-adjustment, amplitude-adjustment, fine-adjustment, tap-adjustment, and voltage division ratio adjustment registers. Each register consists of positive-polarity register and negative-polarity register to allow optimal gamma correction setting for the characteristics of the panel by enabling different settings for positive and negative polarities.

γ Correction registers

The γ-correction registers of the R61509 consists of gradient-adjustment, amplitude-adjustment, fine-adjustment, tap-adjustment, and voltage division ratio adjustment registers to correct grayscale voltage levels according to the gamma characteristics of the liquid crystal panel. These register settings make adjustments to the relationship between grayscale number and grayscale voltage and the setting can be made differently for positive and negative polarities (the reference level and the register settings are the same for all RGB dots). The function of each register is as follows.

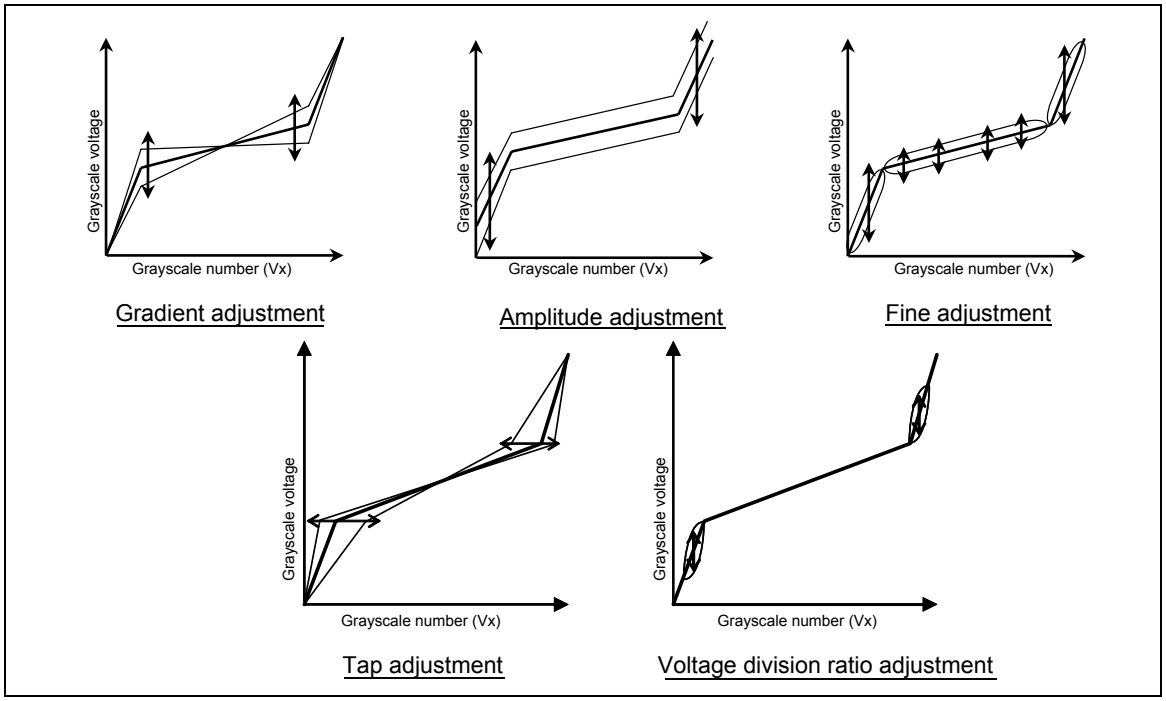


Figure 97

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient, which represents the relationship between grayscale and voltage, without changing the dynamic range. The grayscale voltages for middle grayscale number can be adjusted by this register setting.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage.

3. Fine adjustment registers

The fine adjustment registers are used for minute adjustment of grayscale voltage levels.

4. Tap adjustment registers

The tap adjustment registers are for selecting two tap voltage supply points from V3 to V6 and from V25 to V28 by using selector.

5. Voltage division ratio adjustment registers

The voltage division ratio adjustment registers are used to change the division ratios between V0 and V1 and between V30 and V31.

Table 100 γ correction registers

Register	Positive	Negative	Function
Gradient	P0RP0 [2:0]	P0RN1 [2:0]	Grayscale V4 variable resistance
	P0RP1 [2:0]	P0RN0 [2:0]	Grayscale V27 variable resistance
Amplitude	V0RP0 [4:0]	V0RN1 [4:0]	Voltage level for grayscale V0
	V0RP1 [4:0]	V0RN0 [4:0]	Voltage level for grayscale V31
Fine adjustment	P0KP0 [2:0]	P0KN5 [2:0]	Voltage level for grayscale V1
	P0KP1 [2:0]	P0KN4 [2:0]	Voltage level for grayscales V3, V4, V5, V6
	P0KP2 [2:0]	P0KN3 [2:0]	Voltage level for grayscale V10
	P0KP3 [2:0]	P0KN2 [2:0]	Voltage level for grayscale V21
	P0KP4 [2:0]	P0KN1 [2:0]	Voltage level for grayscales V28, V27, V26, V25
	P0KP5 [2:0]	P0KN0 [2:0]	Voltage level for grayscales V30
	P0FP0 [1:0]	P0FN3 [1:0]	Division ratio between V0 and V1
	P0FP1 [1:0]	P0FN2 [1:0]	P0FP1[1:0]: specify grayscale for P0KP1[2:0] P0FN2[1:0]: specify grayscale for P0KN4[2:0]
	P0FP2 [1:0]	P0FN1 [1:0]	P0FP2[1:0]: specify grayscale for P0KP4[2:0] P0FN1[1:0]: specify grayscale for P0KN1[2:0]
	P0FP3 [1:0]	P0FN0 [1:0]	Division ratio between V30 and V31

γ Correction Register Settings and γ Curve Relationship

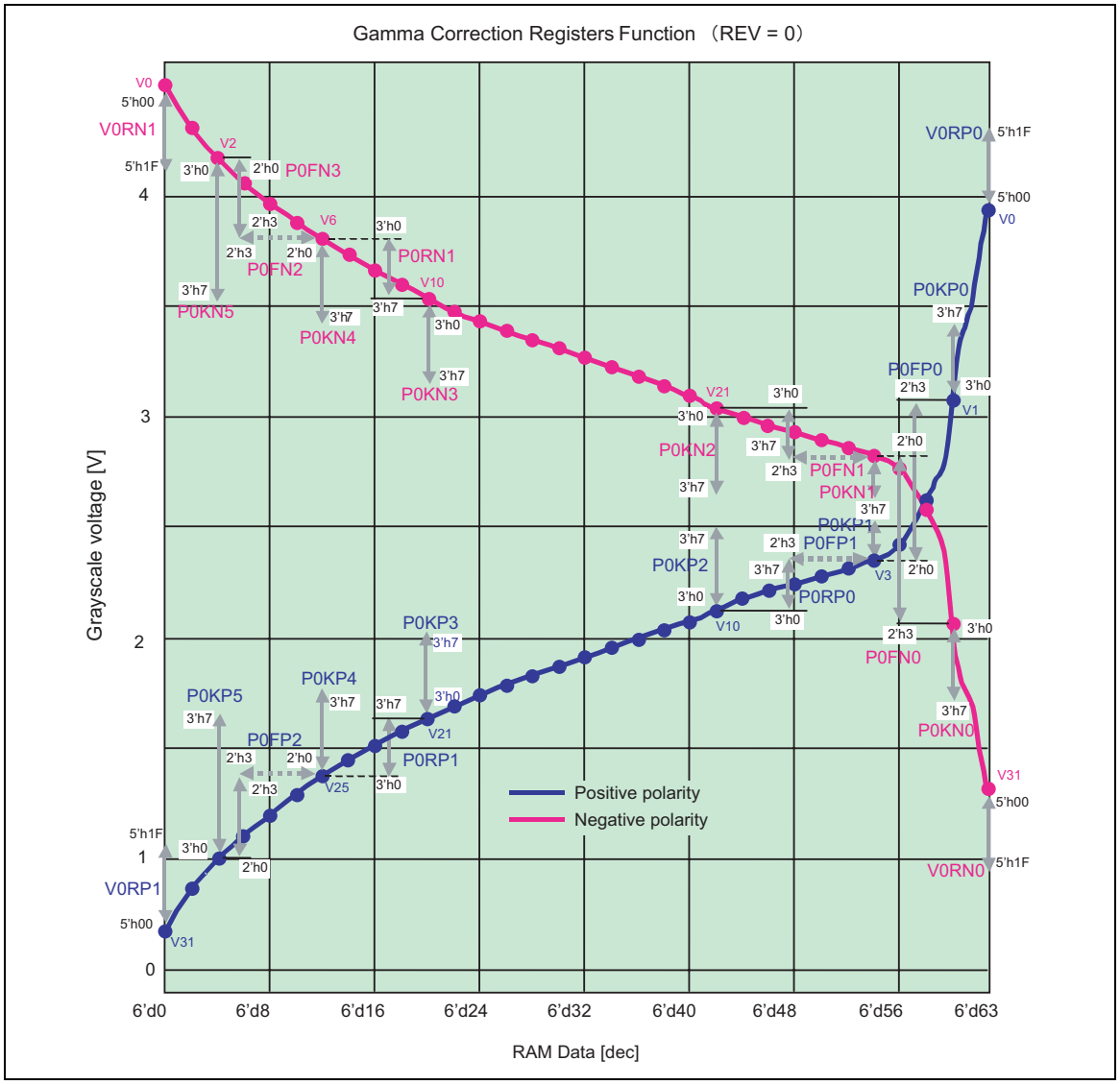


Figure 98

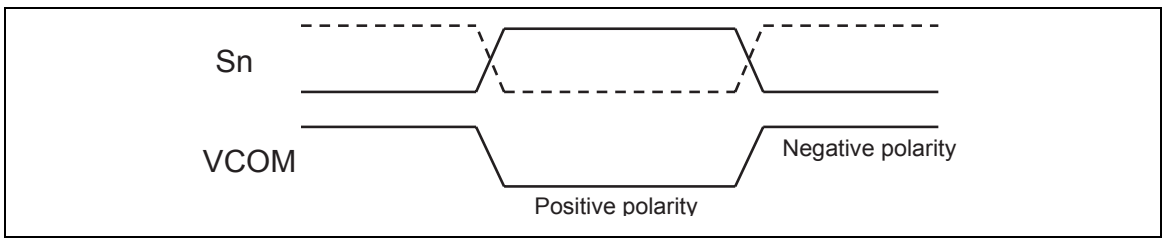


Figure 99 Source Output Waveform and VCOM Polarity Relationship

Power Supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the R61509.

Power Supply Circuit Connection Example 1 (VCI1 = VCIOUT)

In the following example, the VCIOUT level is adjusted internally in the VCIOUT output circuit.

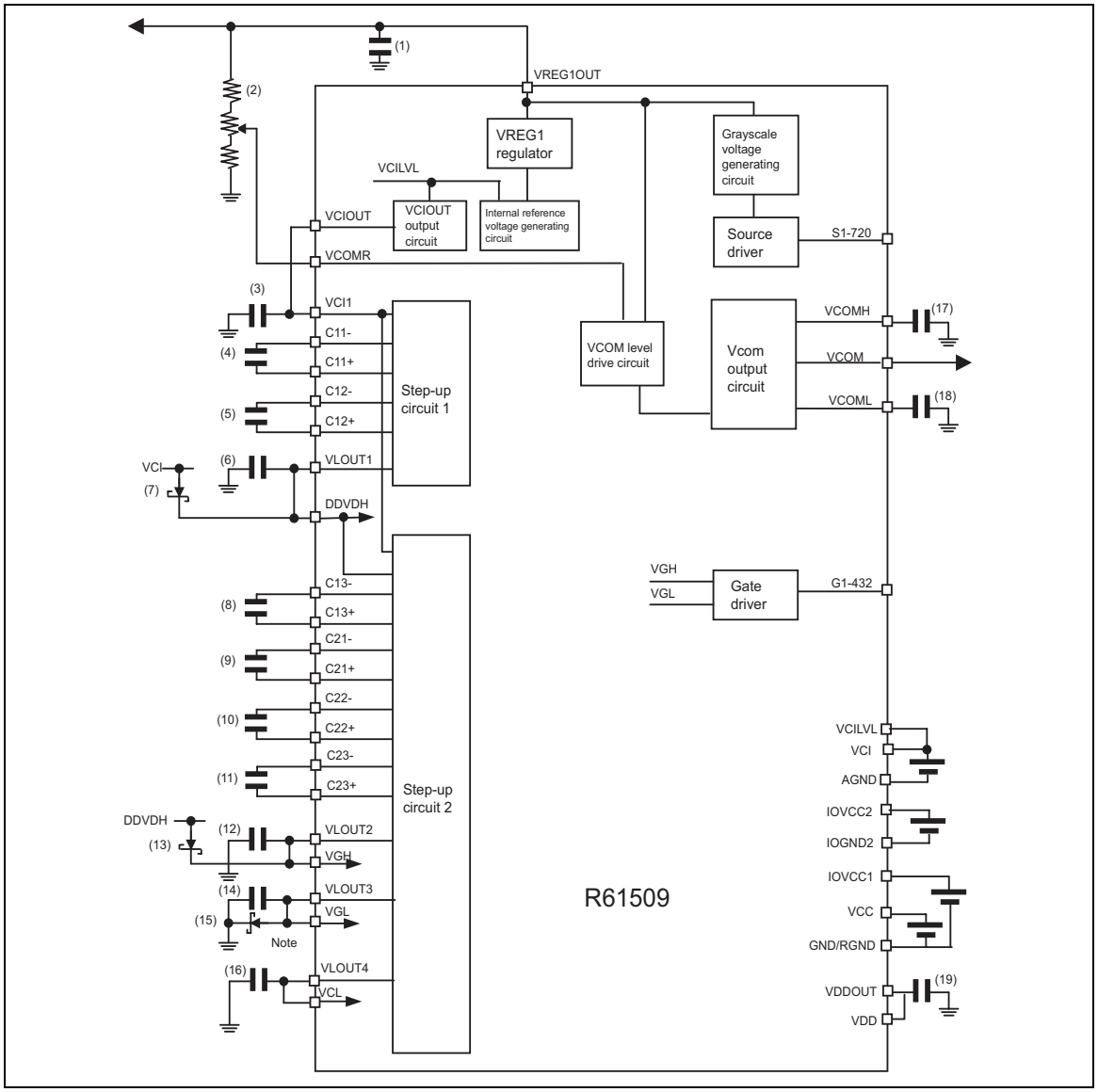


Figure 100

Note: The wiring resistances between the schottky diode and GND/VGL must be 10Ω or less.

Power Supply Circuit Connection Example 2 (VCI1 = VCI direct input)

In the following example, the electrical potential VCI is directly applied to VCI1. In this case, the VCIOUT level cannot be adjusted internally but step-up operation becomes more effective. Make sure that VCI≤ 3.0V.

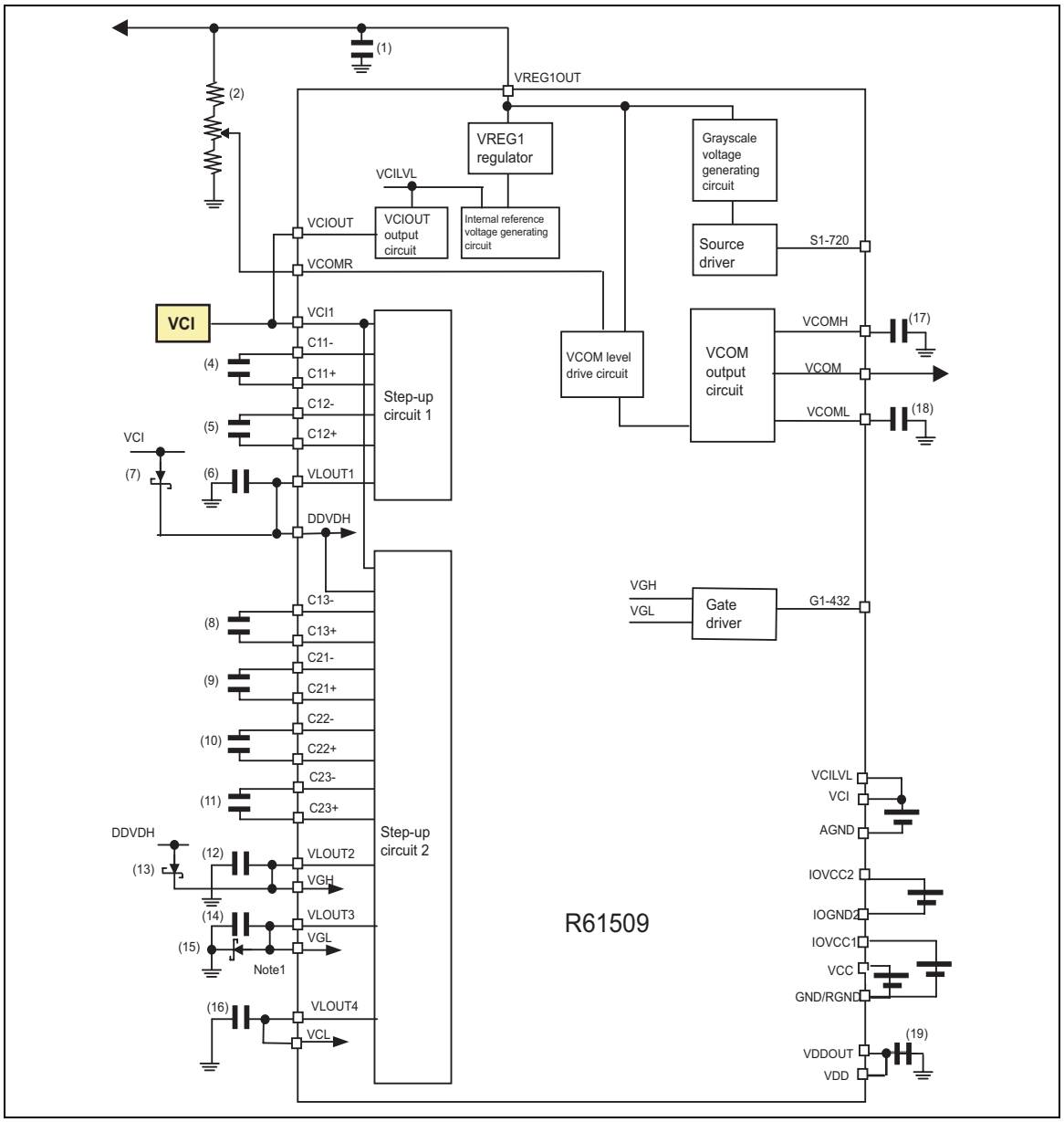


Figure 101

Notes: 1. The wiring resistances between the schottky diode and GND/VGL must be 10Ω or less.

2. When directly applying the VCI level to VCI1, set VC = 3'h7. Capacitor connection to VCIOUT is not necessary.

Specifications of Power-supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the R61509 are as follows.

Table 101 Capacitor

Capacitance	Voltage proof	Pin Connection
1µF (B characteristics)	6 V	(1) VREG1OUT, (3) VCIOUT, (4) C11-/+, (5) C12-/+, (8) C13-/+, (16) VLOUT4, (17) VCOMH, (18)VCOML
	10 V	(6) VLOUT1, (9) C21-/+, (10) C22-/+, (11) C23-/+
	25 V	(11) VLOUT2, (14) VLOUT3

Table 102 Schottky Diode

Specification	Pin Connection
VF < 0.4 V/20 mA@25 °C, VR ≥ 25 V (Recommended diode: HS*226)	(15) GND–VGL, (13) DDVDH–VGH, (7) VCI–DDVDH

Table 103 Variable Resistor

Specification	Pin Connection
> 200 kΩ	(2) VCOMR

Table 104 Internal Logic Power Supply

Capacitance	Voltage proof (recommended)	Pin Connection
1µF (B characteristics)	3V	(19) VDD

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61509 and the TFT display application voltage waveforms and electrical potential relationship.

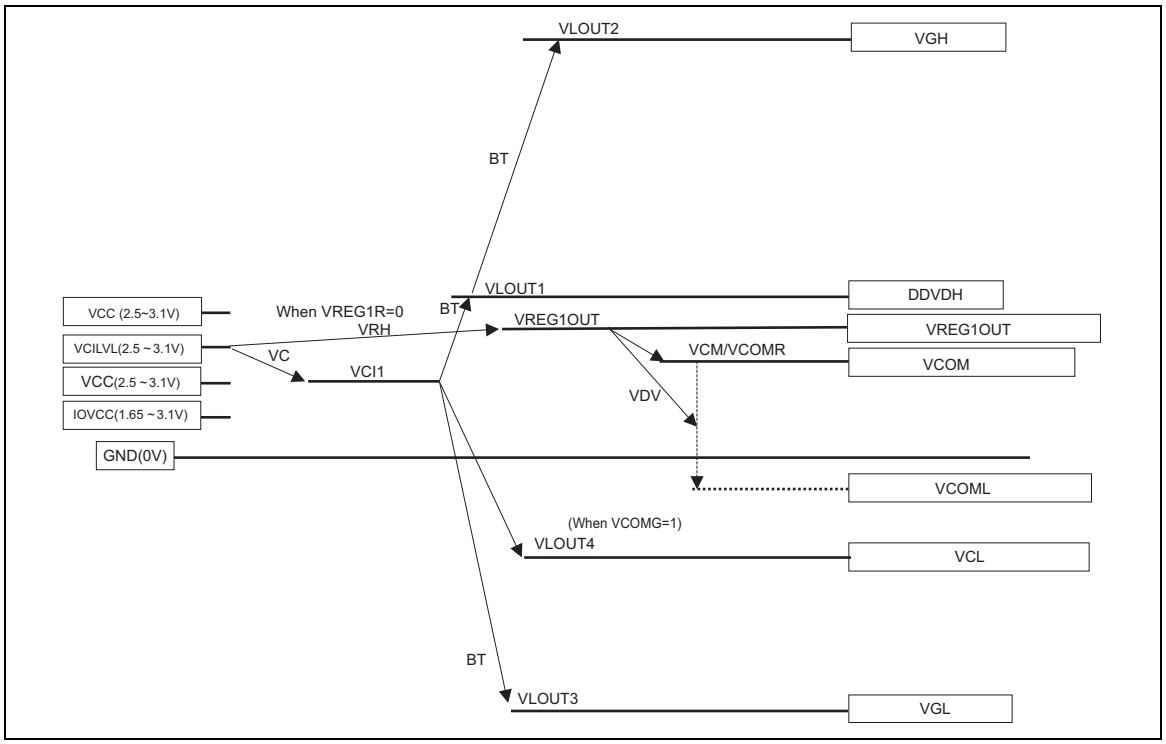


Figure 102

Notes: 1. The DDVDH, VGH, VGL, and VCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at each output level. Make sure that output voltage level in operation maintains the following relationships: (DDVDH – VREG1OUT) > 0.5V, (VCOML – VCL) > 0.5V. Also make sure VGH-VGL ≤ 28V, VCI-VCL ≤ 6V. When the alternating cycle of VCOM is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

2. In operation, setting voltages within the respective voltage ranges is recommended.

Liquid crystal application voltage waveform and electrical potential

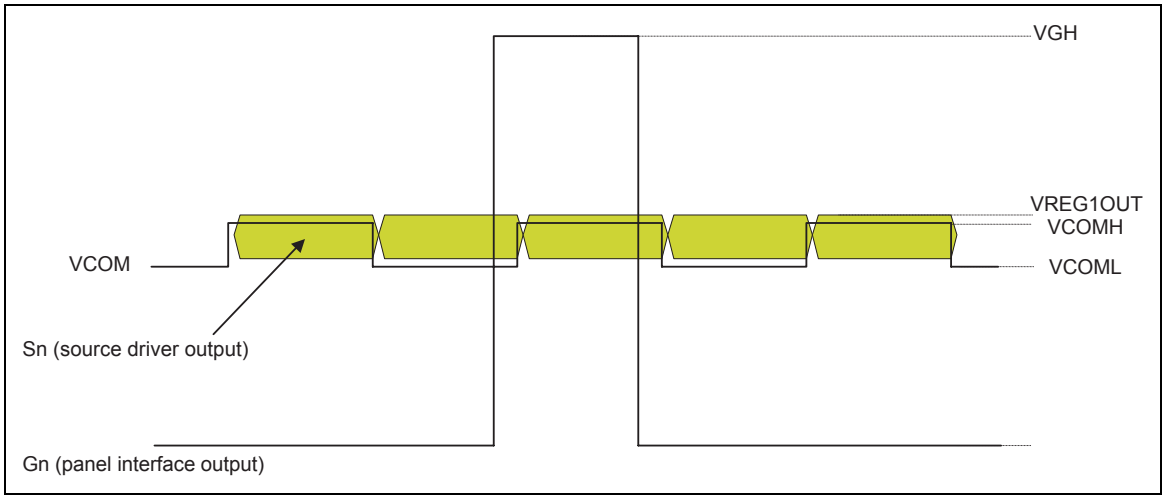


Figure 103

VCOMH voltage adjustment sequence

When adjusting the VCOMH voltage by setting VCM1[5:0] (R281h, internal VCOMH level adjustment circuit), follow the sequence below. The R61509 can retain the VCOMH level adjustment setting values in NVM, which allows writing twice (only one setting value can be written in NVM at one time).

Set write data to VCM1[4:0] (R281h), VCMSEL and VCM2 [4:0] (R282h) to write to NVM. See "NVM Control Sequence".

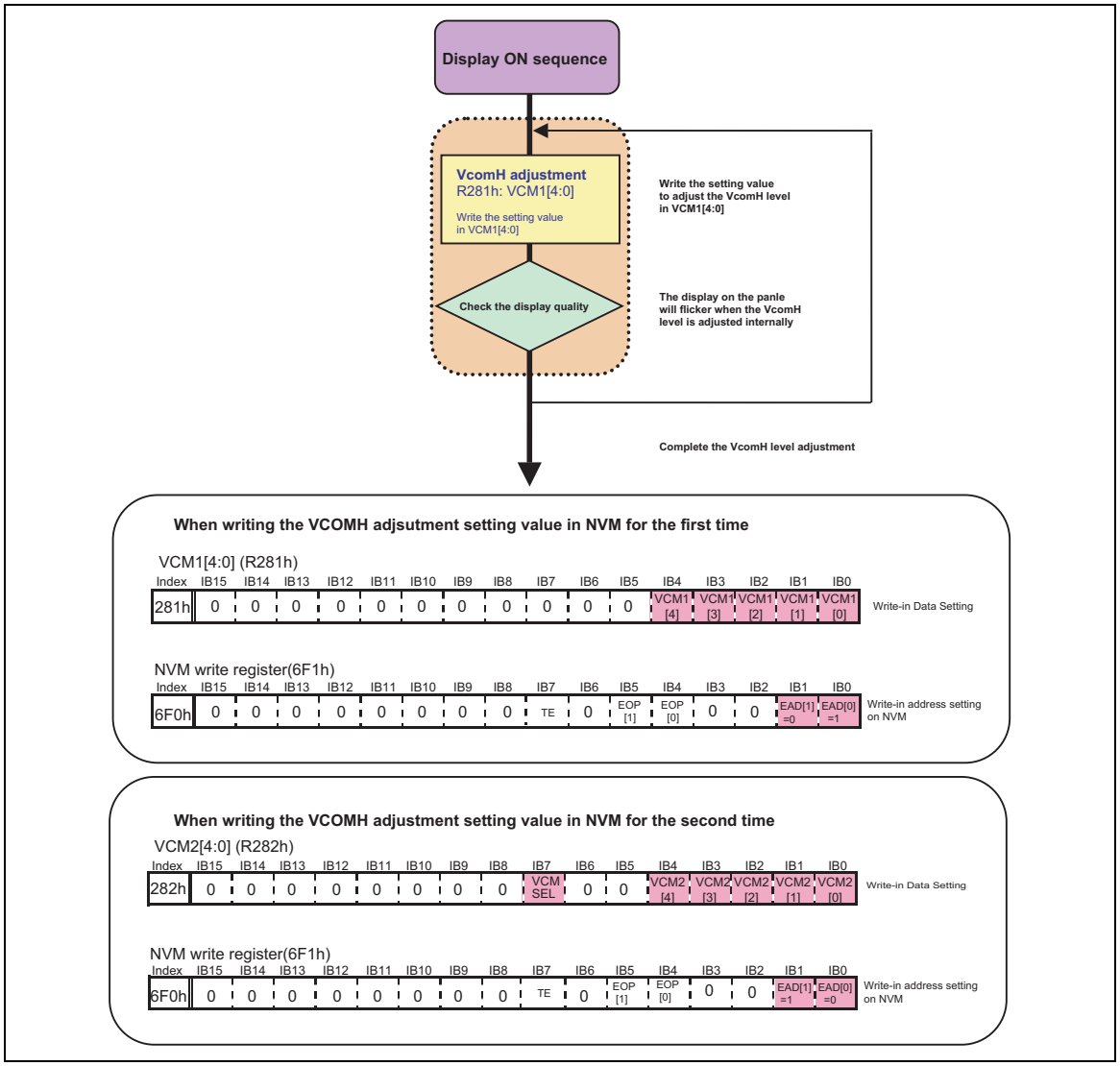


Figure 104

NVM Control Sequence

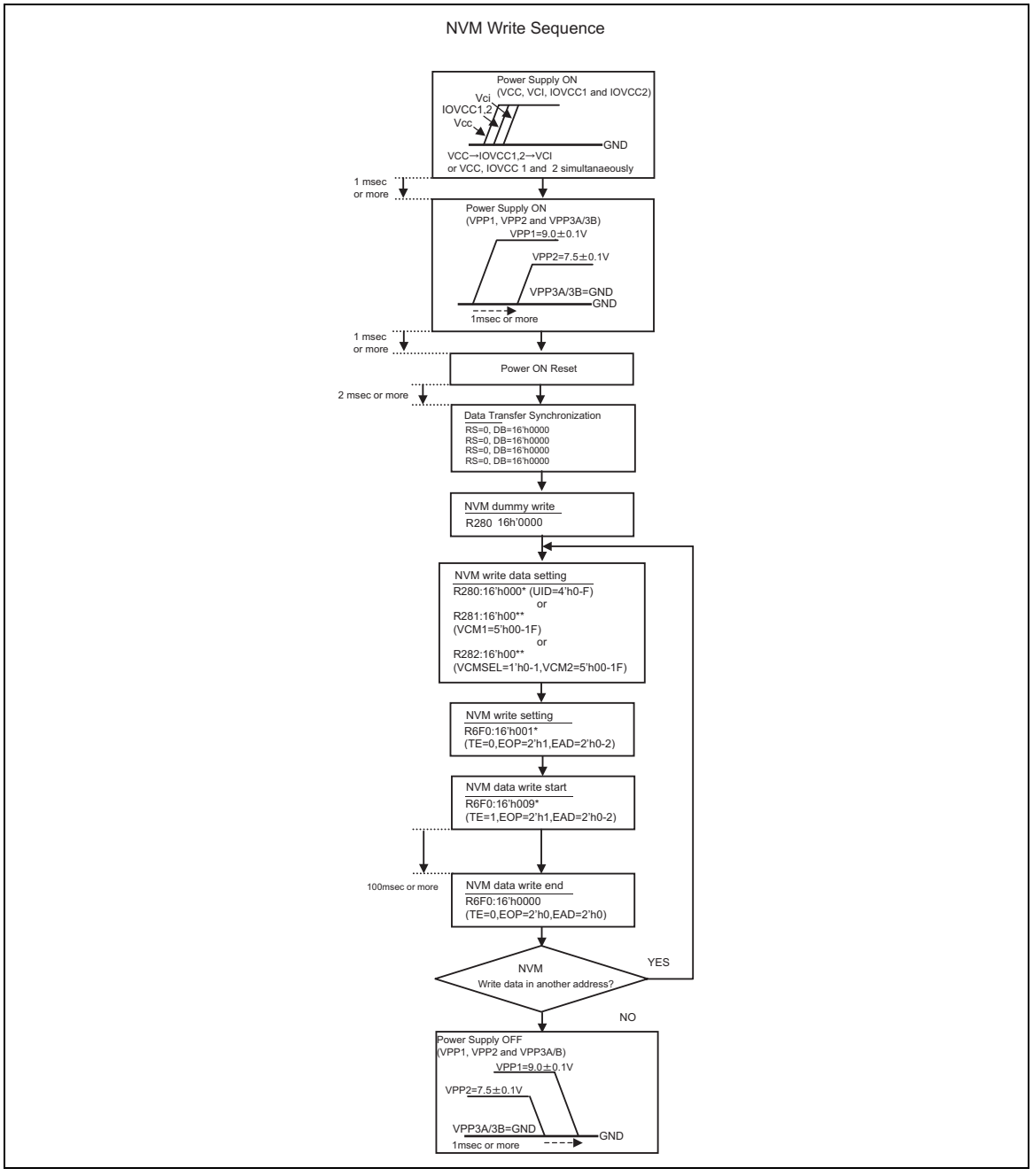


Figure 105

NVM Instruction Dummy Read Sequence

In accessing NVM instruction registers (R280, R281, R282, R6F0, R6F1, and R620), perform dummy write or dummy read. In dummy write operation, write data on the same index. NVM instruction registers can be accessed consecutively by performing a dummy access at first.

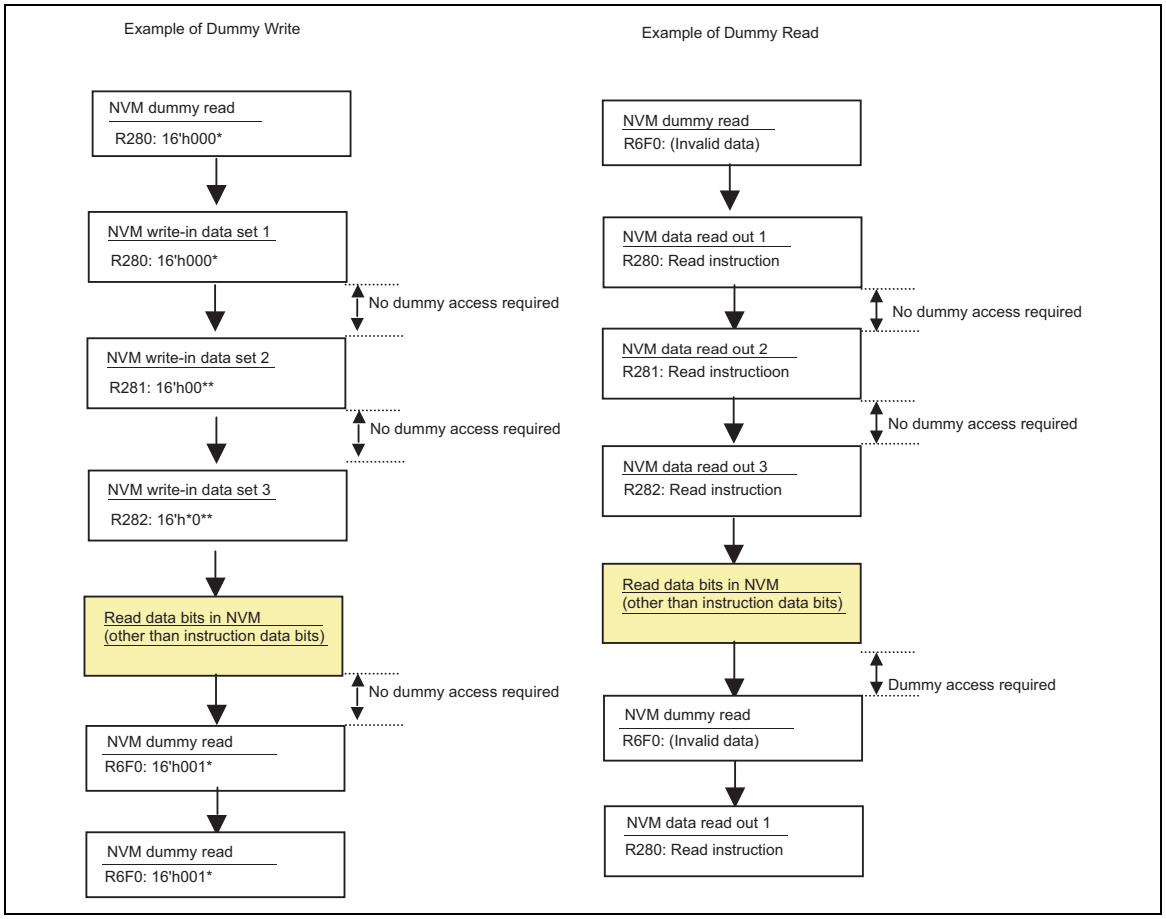


Figure 106

Power Supply Instruction Setting

The following are the sequences for setting power supply ON/OFF instructions. Set power supply ON/OFF instructions according to the following sequences in Display ON/OFF, Sleep set/exit sequences. Do not execute a hardware reset without Power supply OFF sequence. If not, electrical power may not be discharged properly.

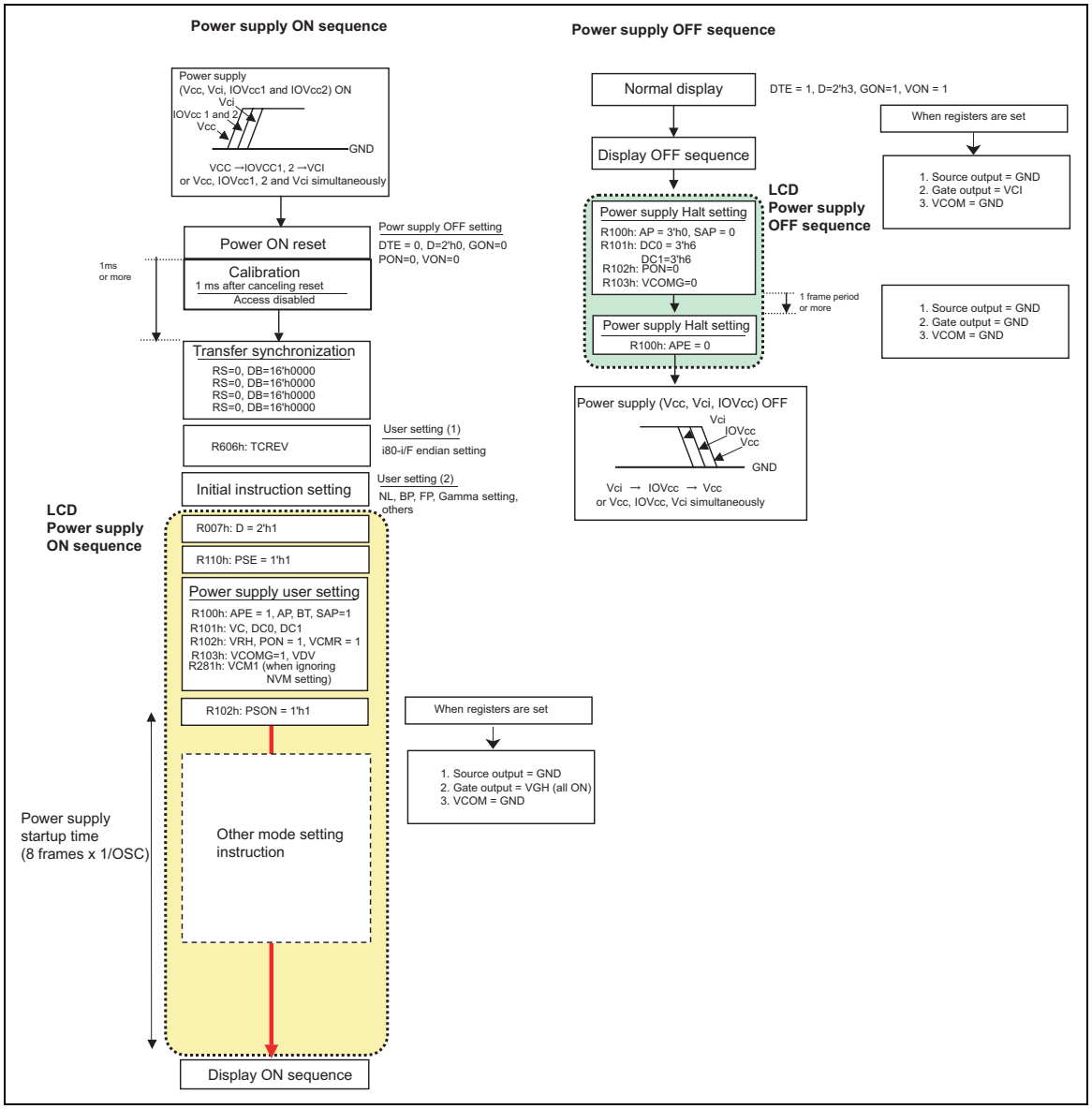


Figure 107

Notes to Power Supply ON Sequence

When voltages do not rise in the order of VCC, IOVCC and then VCI and have to change the order, please follow the following note.

Note

Internal operation of the R61509 is unstable until VCC rises. If IOVCC rose before VCC rises, the R61509 may be in “output” status. In this case, do not send or receive any data before power supply is completed.

Changing order of voltage input will not cause troubles such as latchup or destruction of the LSI.

Instruction Setting

The following are the sequences for various instruction settings. When setting instruction in the R61509, follow the relevant sequence below.

Display ON/OFF Sequences

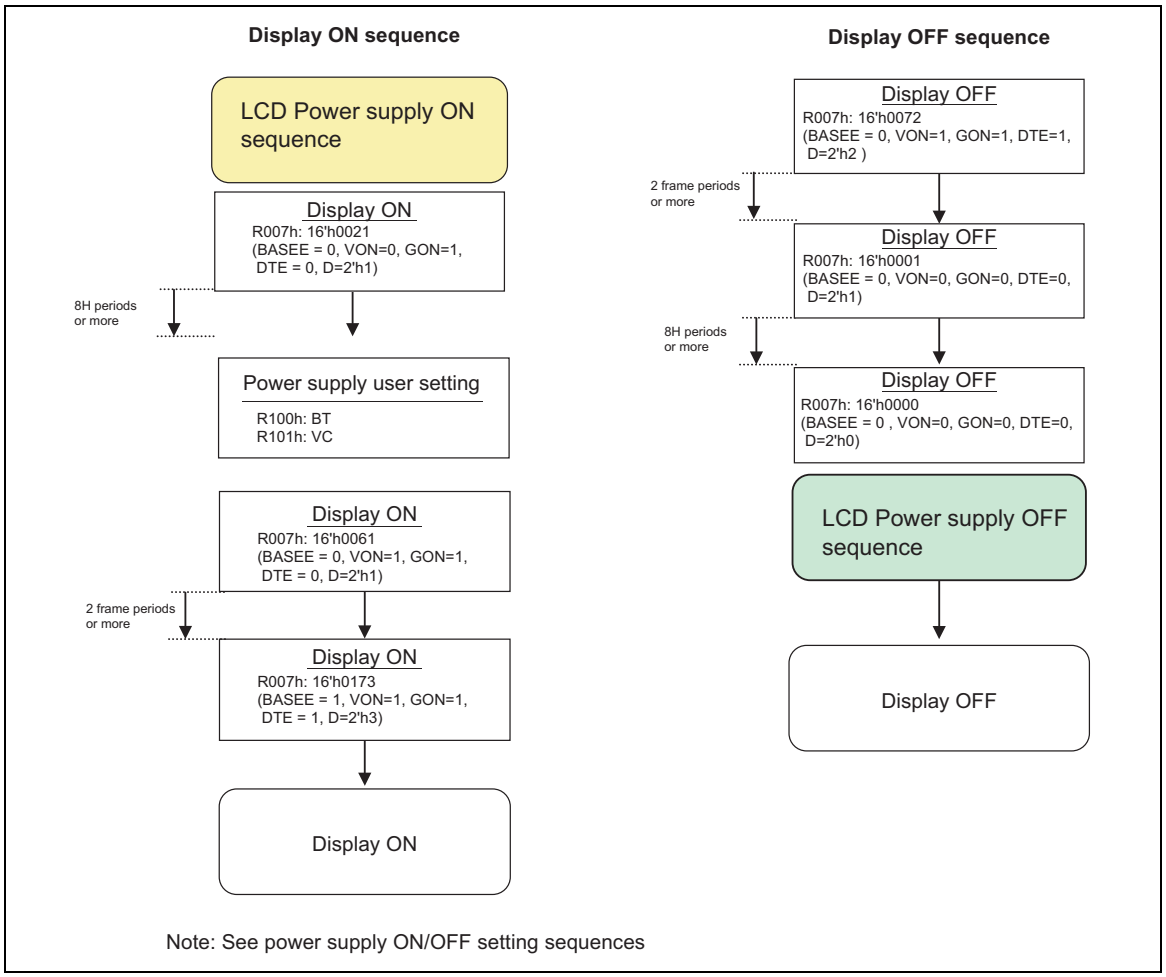


Figure 108

Sleep Mode SET/EXIT Sequences

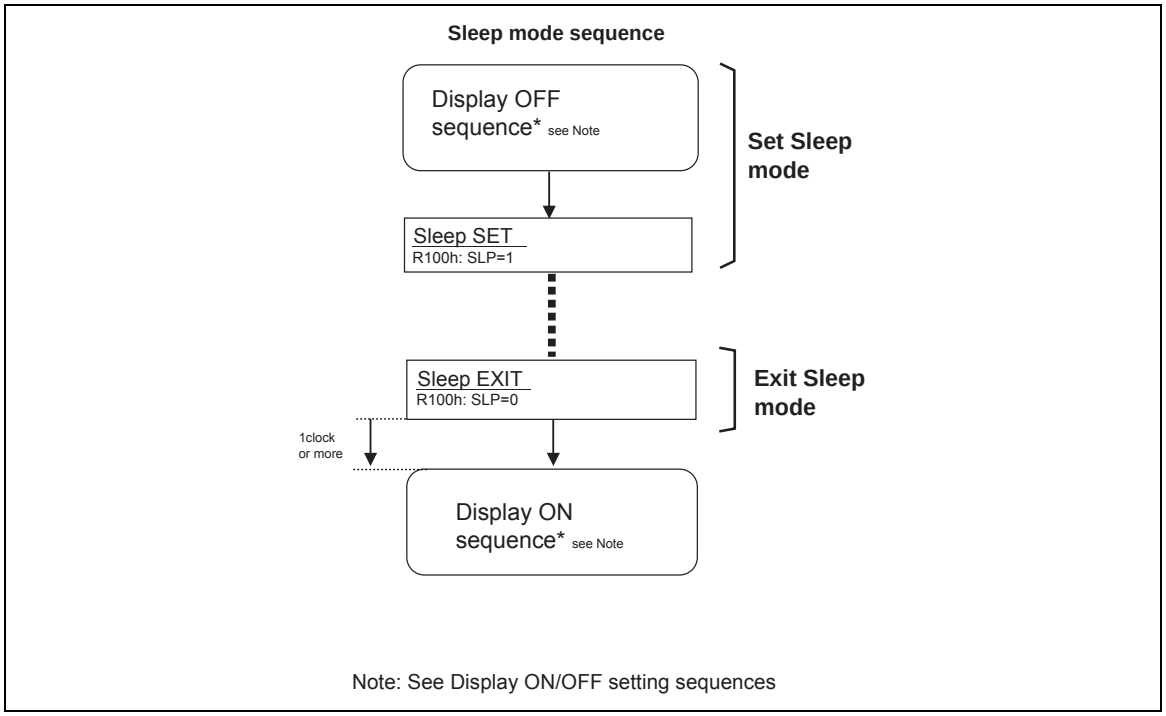


Figure 109

Shutdown Mode IN/EXIT Sequences

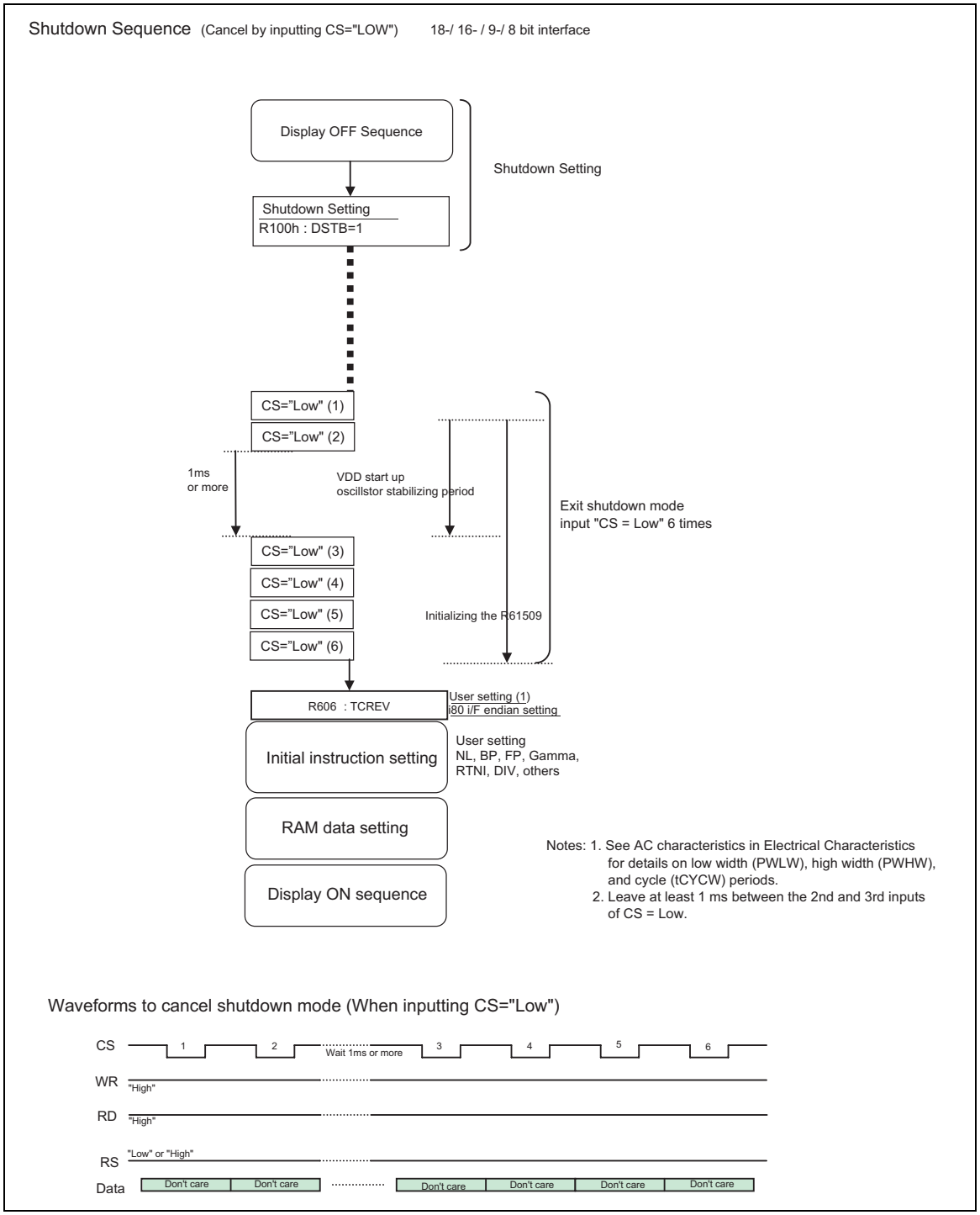


Figure 110

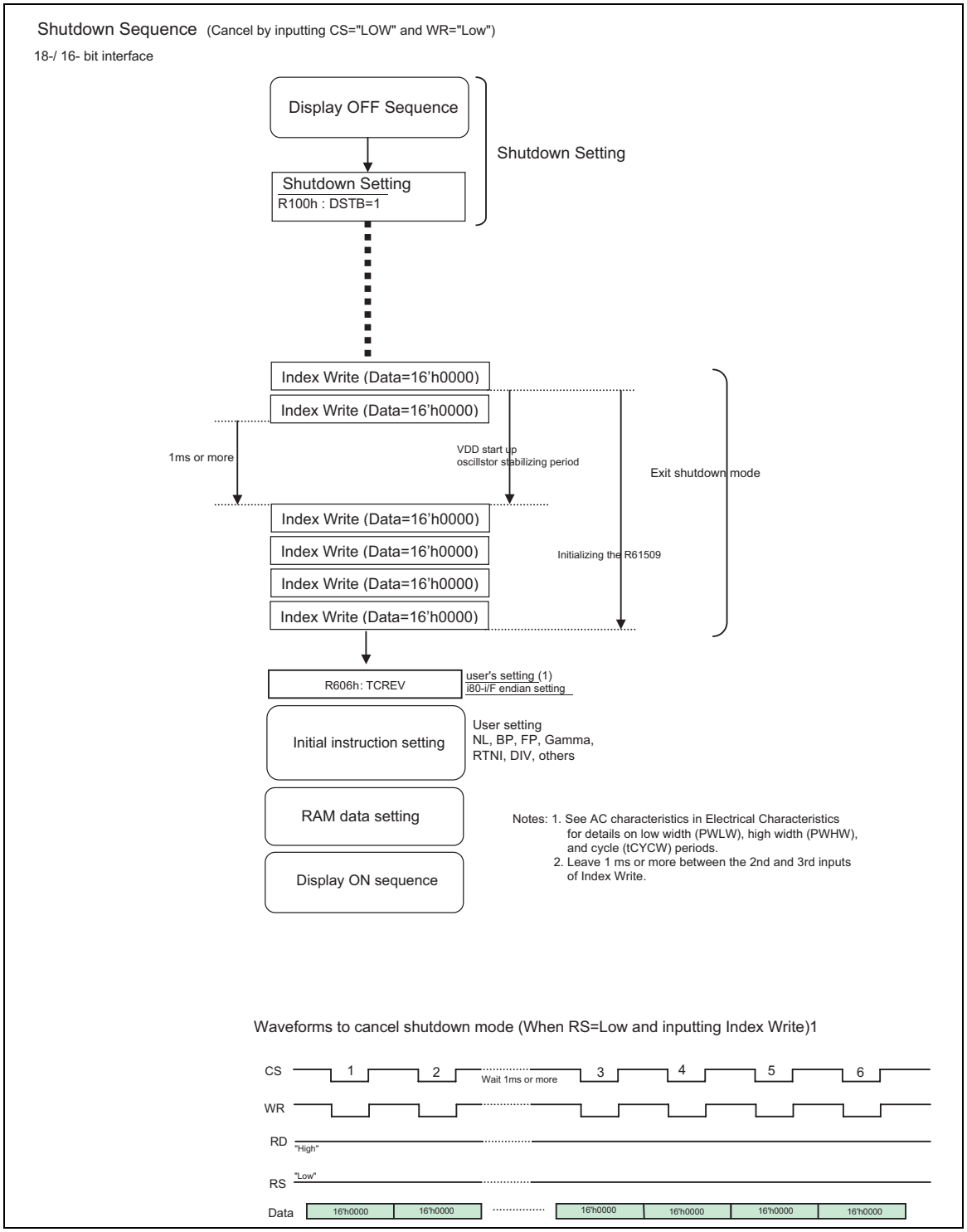

Shutdown Sequence (Cancel by inputting CS="LOW" and WR="Low")
18-/ 16- bit interface
Display OFF Sequence
Shutdown Setting
Shutdown Setting
R100h : DSTB=1
Index Write (Data=16'h0000)
Index Write (Data=16'h0000)
1ms or more
VDD start up
oscillstor stabilizing period
Exit shutdown mode
Index Write (Data=16'h0000)
Index Write (Data=16'h0000)
Initializing the R61509
Index Write (Data=16'h0000)
Index Write (Data=16'h0000)
R606h: TCREV
user's setting (1)
i80-i/F endian setting
Initial instruction setting
User setting
NL, BP, FP, Gamma,
RTNI, DIV, others
RAM data setting
Display ON sequence
Notes: 1. See AC characteristics in Electrical Characteristics
for details on low width (PWLW), high width (PWHW),
and cycle (tCYCW) periods.
2. Leave 1 ms or more between the 2nd and 3rd inputs
of Index Write.
Waveforms to cancel shutdown mode (When RS=Low and inputting Index Write)1
CS
WR
RD
RS
Data
1
2
3
4
5
6
Wait 1ms or more
"High"
"Low"
16'h0000
16'h0000
16'h0000
16'h0000
16'h0000
16'h0000

Figure 111

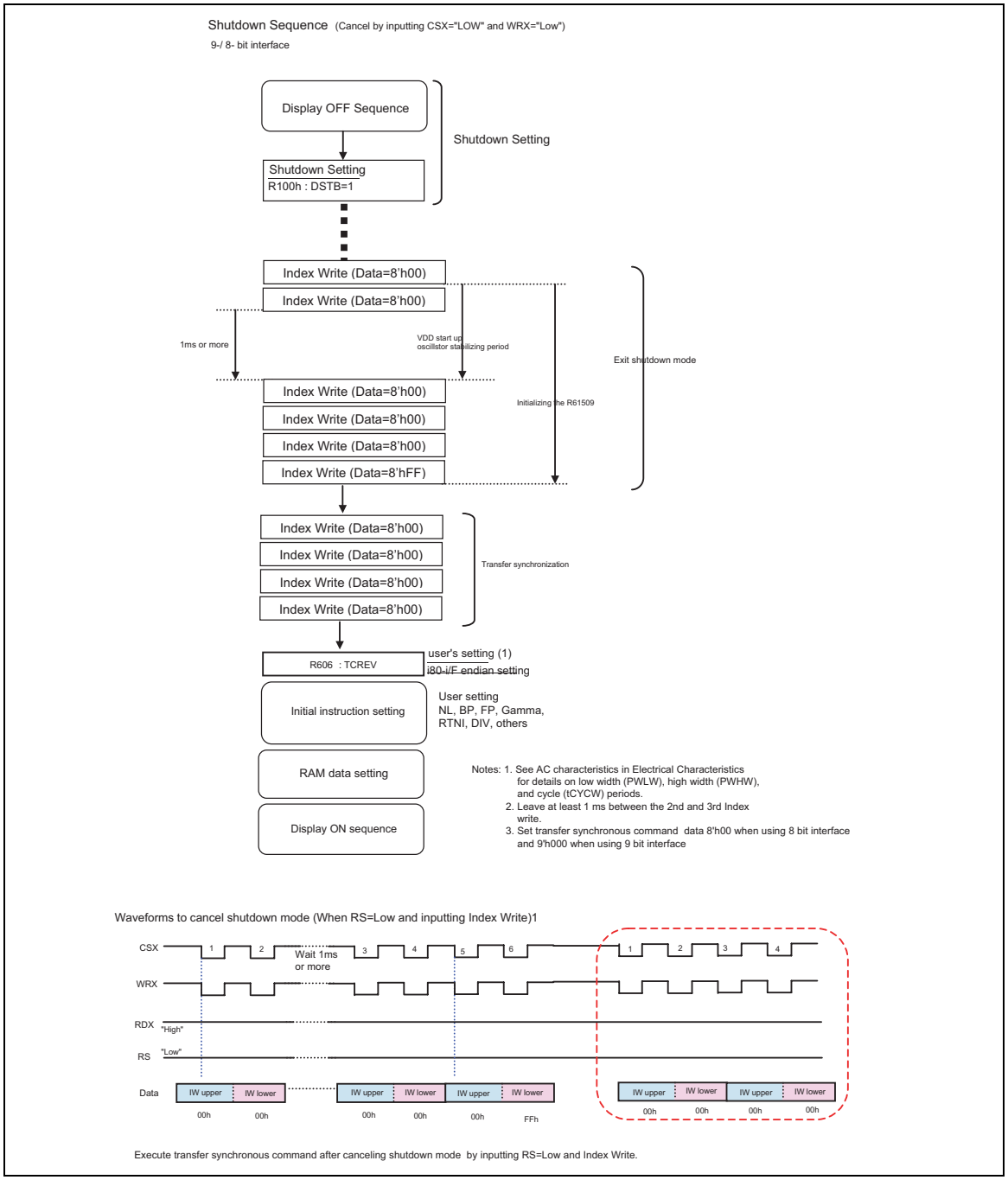

Shutdown Sequence (Cancel by inputting CSX="LOW" and WRX="Low")
9-/ 8- bit interface
Display OFF Sequence
Shutdown Setting
Shutdown Setting
R100h : DSTB=1
Index Write (Data=8'h00)
Index Write (Data=8'h00)
1ms or more
VDD start up
oscillstor stabilizing period
Exit shutdown mode
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Index Write (Data=8'hFF)
Initializing the R61509
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Transfer synchronization
R606 : TCREV
user's setting (1)
i80-i/F endian setting
Initial instruction setting
User setting
NL, BP, FP, Gamma,
RTNI, DIV, others
RAM data setting
Display ON sequence
Notes: 1. See AC characteristics in Electrical Characteristics
for details on low width (PWLW), high width (PWHW),
and cycle (tCYCW) periods.
2. Leave at least 1 ms between the 2nd and 3rd Index
write.
3. Set transfer synchronous command data 8'h00 when using 8 bit interface
and 9'h000 when using 9 bit interface
Waveforms to cancel shutdown mode (When RS=Low and inputting Index Write)1
CSX
WRX
RDX
RS
Data
"High"
"Low"
Wait 1ms
or more
IW upper
IW lower
00h
FFh
Execute transfer synchronous command after canceling shutdown mode by inputting RS=Low and Index Write.

Figure 112

8-Color Mode Setting

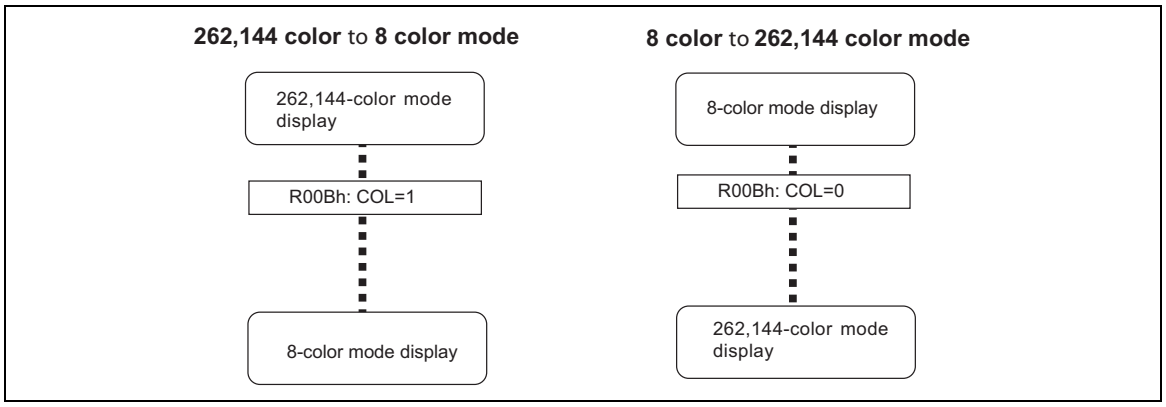


Figure 113

Partial Display Setting

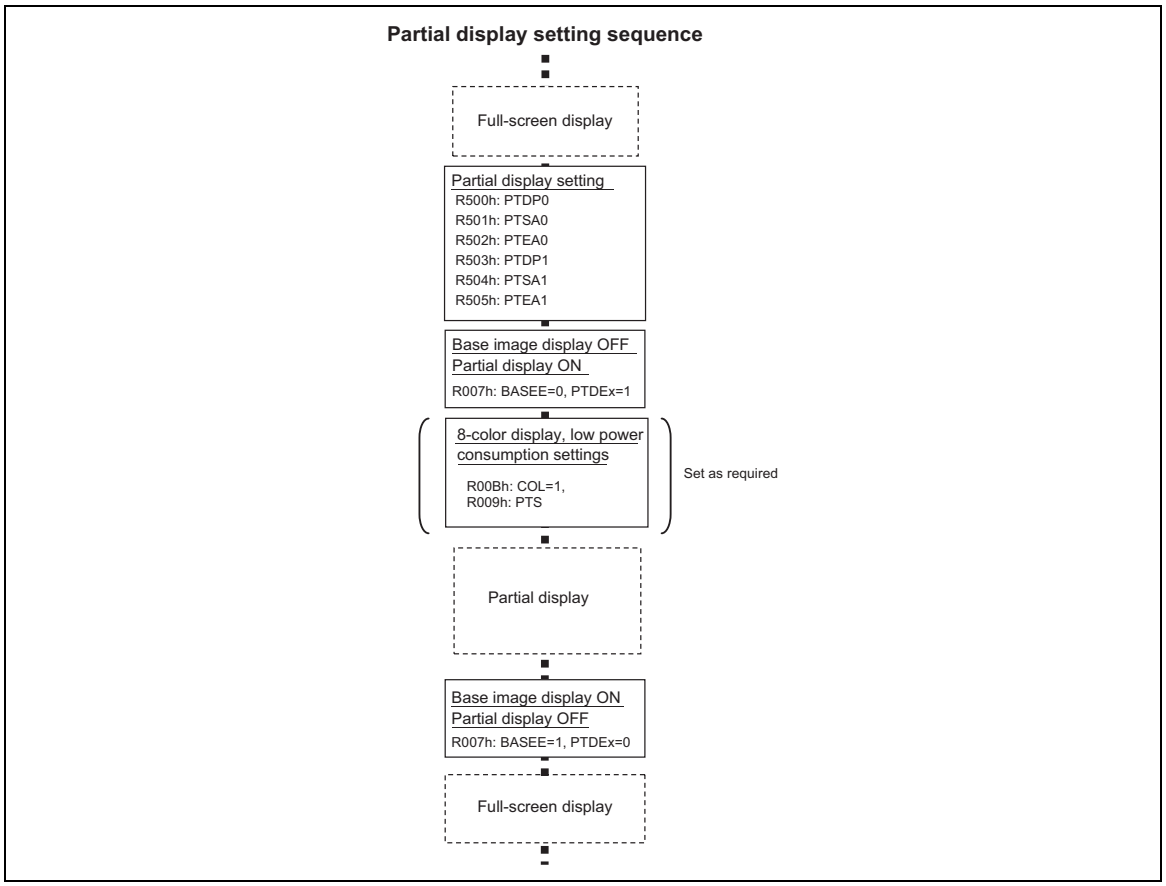


Figure 114

Absolute Maximum Ratings

Table 105

Items	Symbol	Unit	Value	Note
Power supply voltage 1	VCC, IOVCC1, IOVCC2	V	-0.3 ～ +4.6	1, 2
Power supply voltage 2	VCI – AGND	V	-0.3 ～ +4.6	1, 3
Power supply voltage 3	DDVDH – AGND	V	-0.3 ～ +6.5	1, 4
Power supply voltage 4	AGND – VCL	V	-0.3 ～ +4.6	1
Power supply voltage 5	DDVDH – VCL	V	-0.3 ～ +9.0	1, 5
Power supply voltage 7	AGND– VGL	V	-0.3 ～ +13.0	1, 6
Power supply voltage 8	VGH– VGL	V	-0.3 ～ 30.0	1
Power supply voltage 9	VPP1	V	-0.3 ～ +10.0	1
Power supply voltage 10	VPP2	V	-0.3 ～ +10.0	1
Power supply voltage 11	VPP3A/VPP3B	V	0	1
Input voltage	Vt	V	-0.3 ～ IOVCC1 + 0.3	1
Operation temperature	Topr	℃	-40 ～ +85	1, 7
NVM write temperature	Twep	℃	+25 ～ +35	1
Storage temperature	Tstg	℃	-55 ～ +110	1

Note1: If used beyond the absolute maximum ratings, the LSI may be permanently damaged. It is strongly recommended to use the LSI under the condition within the electrical characteristics in normal operation. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

Note 2: Make sure VCC≥GND, IOVCC1≥GND and IOVCC2≥IOGND2.

Note 3: Make sure VCI≥AGND.

Note 4: Make sure DDVDH ≥ AGND.

Note 5: Make sure DDVDH≥VCL.

Note 6: Make sure AGND≥VGL.

Note 7: The DC/AC characteristics of the die and wafer products are guaranteed at 85℃.

Electrical Characteristics

DC Characteristics

（VCC= 2.50V～3.10V，IOVCC1=1.65V～3.10V，Ta= -40℃～+85℃ Note 1）

Table 106

Items	Symbol	Unit	Test condition	Min.	Typ.	Max.	Notes
Input high-level voltage	V_{IH}	V	IOVCC=1.65V～3.10V	0.80× IOVCC1	–	IOVCC1	2, 3
Input low-level voltage	V_{IL}	V	IOVCC=1.65V～3.10V	-0.3	–	0.20× IOVCC1	2, 3
Output high voltage 1 （DB0-17,FMARK）	V_{OH1}	V	IOVCC=1.65V～3.10V, IOH=-0.1mA	0.8× IOVCC	–	–	2
Output low voltage 1 （DB0-17,FMARK）	V_{OL1}	V	IOVCC=1.65V～3.10V, IOL=0.1mA	–	–	0.20× IOVCC1	2
I/O leakage current (Except MDDI_STB_* and MDDI_DATA_*)	I_{LI1}	μA	Vin=0～IOVCC1	-1	–	1	4
I/O leakage current (except MDDI_STB_* and MDDI_DATA_*)	I_{LI2}	μA	Vin=0～IOVCC2	-1	–	1	4
Current consumption ((IOVCC-IOGND)+ (VCC-GND)) Normal operation mode (260k colors, display operation)	I_{OP1}	μA	fosc=678kHz (432 line drive), I80-IF, IOVCC1=VCC=3.00V, fFLM=60Hz, Ta=25℃, RAM data: 18'h000000, See other as well.	–	175	400	5, 6
Current consumption ((IOVCC-IOGND)+ (VCC-GND)) 8-color, 64-line partial display on sub display	I_{op2}	μA	fosc=678kHz (64 line partial display), IOVCC1=VCC=3.00V, fFLM=40Hz, Ta=25℃, RAM data: 18h'000000, see other as well.	–	100	–	5, 6
Current consumption ((IOVCC-IOGND)+ (VCC-GND)) Shutdown mode	I_{shut1}	μA	IOVCC1=IOVCC2=VCC=3.00V, I80-IF, Ta=25℃	–	0.1	1.0	5
Current consumption ((IOVCC-IOGND)+ (VCC-GND)) RAM access mode 1 (Normal write operation (HWM=0))	I_{RAM1}	mA	IOVCC1=2.40V, VCC=3.00V, tCYCW=110ns, Ta=25℃, I80-8bit-I/F, TRIREG=1'h1, Consecutive RAM access during display operation, BC0=0, FP=5, BP=8, γ register; 0(default), COL=0	–	2.8	–	6
Current consumption ((IOVCC-IOGND)+ (VCC-GND)) RAM access mode 2 (High-speed write function (HWM=1))	I_{RAM2}	mA	IOVCC1=2.40V, VCC=3.00V, tCYCW=60ns, Ta=25℃, I80-8bit-I/F, TRIREG=1'h1, Consecutive RAM access during display operation, BC0=0, FP=5, BP=8, γ register; 0(default), COL=0	–	1.5	–	6
LCD power supply current (VCI-GND) 260k-color display	Ici1	mA	IOVCC1=VCC=3.00V, VCI=3.0V, fosc=678kHz (432 line), fFLM=60Hz, Ta=25℃, RAM data: 18'h00000, REV0="0", BC0=0, FP=5, BP=8, V0RPx="0", V0RNx="0", P0KPx="0", P0KNx="0", P0RPx="0", P0RNx="0", P0FPx="0", P0FNx="0", BT=3'h6, VC=3'h1, AP=3'h3, DC0=3'h1, DC1=3'h2, VRH=4'hA, VCM1=5'h1D, VDV=5'h1A, VCMR=1'h1, COL=0, GON=1, No load on the panel.	–	2.0	3.0	5, 6

LCD power supply current (VCI-GND) 8-color, 64-line partial display	Ici2	mA	IOVCC1=VCC= 3.00V, VCI=3.0V, fosc=678kHz (64 line partial display), fFLM=40Hz, Ta=25℃, RAM data: 18'h00000, REV0="0", BC0=0, FP=5, BP=8, V0RPx="0", V0RNx="0", P0KPx="0", P0KNx="0", P0RPx="0", P0RNx="0", P0FPx="0", P0FNx="0", BT=3'h6, VC=3'h1, AP=3'h3, DC0=3'h2, DC1=3'h2, VRH=4'hA, VCM1=5'h1D, VDV=5'h1A, VCMR=1'h1, COL=1, GON=1, No load on the panel.	–	0.38	–	5, 6
Output voltage dispersion	ΔVO	mV	–	–	5	–	7
Average output variance	ΔVΔ	mV	–	−35	–	35	8

MDDI DC Characteristics

(IOVCC1=1.65V～3.10V, VCC=IOVCC2=2.5V～3.10V, Ta= -30℃～+85℃ Note 1)

Table 107

Items	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Differential input "High" threshold voltage (VT=0) (MDDI_DATA_P/M, MDDI_STB_P/M)	VIT+	mV		–	0	50	-
Differential input "Low" threshold voltage (VT=0) (MDDI_DATA_P/M, MDDI_STB_P/M)	VIT-	mV		-50	0	–	-
Differential input "High" threshold voltage (VT=125mV) (MDDI_DATA_P/M)	VIT+off	mV		–	125	195	-
Differential input "Low" threshold voltage (VT=125mV) (MDDI_DATA_P/M)	VIT- off	mV		75	125	–	-
Input voltage range	VIRNG	V		0	–	1.65	-
Current consumption (IOVCC2-IOGND2) In Hibernation state	I_{hib}	uA	IOVCC1=IOVCC2=VCC=3.0V, $1/t_{BIT}$=70Mbps, Ta=25℃, DFM=0	–	20	–	-
Current consumption (IOVCC2-IOGND2) during data transfer	I_{trans}	mA	IOVCC1=IOVCC2=VCC=3.0V, in video stream packet transfer, $1/t_{BIT}$=70Mbps, Ta=25℃, DFM=0	–	0.4	–	-

Step-up Circuit Characteristics

Table 108

Item		Unit	Test condition	Min.	Typ.	Max.	Note
Step-up output voltage	VLOUT1	V	IOVCC1=IOVCC2=VCC=VCI=3.00[V], fosc=678[kHz], Ta=25℃, VC=3'h1, AP=3'h3, BT=3'h6, DC0=3'h2 (div. 1/4), DC1=3'h2 (div. 1/64), COL=0, D=2'h0, VON=0, C11=C12=C13=C21=C22=C23=1[uF]/B characteristics, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1[uF]/B characteristics, Iload1=−3 [mA], No load on the panel.	4.84	5.14	−	−
	VLOUT2	V	IOVCC1=IOVCC2=VCC=VCI=3.00[V], fosc=678[kHz], Ta=25℃, VC=3'h1, AP=3'h3, BT=3'h6, DC0=3'h2 (div. 1/4), DC1=3'h2 (div. 1/64), COL=0, D=2'h0, VON=0, C11=C12=C13=C21=C22=C23=1[uF]/B characteristics, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1[uF]/B characteristics, Iload2=−100[uA], No load on the panel.	14.47	15.39	−	−
	VLOUT3	V	IOVCC1=IOVCC2=VCC=VCI=3.00[V], fosc=678[kHz], Ta=25℃, VC=3'h1, AP=3'h3, BT=3'h6, DC0=3'h2 (div. 1/4), DC1=3'h2 (div. 1/64), COL=0, D=2'h0, VON=0, C11=C12=C13=C21=C22=C23=1[uF]/B characteristics, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1[uF]/B characteristics, Iload3=+100[uA], No load on the panel.	−	−9.70	−9.12	−
	VLOUT4	V	IOVCC1=IOVCC2=VCC=VCI=3.00[V], fosc=678[kHz], Ta=25℃, VC=3'h1, AP=3'h3, BT=3'h6, DC0=3'h2 (div. 1/4), DC1=3'h2 (div. 1/64), COL=0, D=2'h0, VON=0, C11=C12=C13=C21=C22=C23=1[uF]/B characteristics, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1[uF]/B characteristics, Iload4=+200[uA], No load on the panel.	−	−2.56	−2.41	−
Input voltage	VCI	V		2.5	−	3.1	−

Internal reference voltage: condition

（VCC= 2.50V～3.10V， Ta=-40℃～+85℃）

Table 109

Item	Symbol	Unit	Min.	Typ.	Max.	Note
Internal reference voltage	VCIR	V	-	2.50	-	12

AC Characteristics

VCC= 2.50V～3.10V, IOVCC1=1.65V～3.10V, Ta= -40℃～+85℃ (See note 1)

Clock characteristics

Table 110

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
RC oscillation clock	f_{osc}	kHz	VCC=IOVCC1= IOVCC2=3.0V	631	678	725	9

80-system Bus interface Timing Characteristics

Table 111 《 [A] 16-/18- bit, Normal write mode (HWM=0), IOVCC1=1.65V～3.10V》

Items		Symbol	Unit	Test condition	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	Figure A	110	—	—
	Read	t_{CYCR}	ns	Figure A	450	—	—
Write low- level pulse width		PW_{LW}	ns	Figure A	30	—	—
Read low-level pulse width		PW_{LR}	ns	Figure A	170	—	—
Write high-level pulse width		PW_{HW}	ns	Figure A	30	—	—
Read high-level pulse width		PW_{HR}	ns	Figure A	250	—	—
Write/ Read rise/fall time		t_{WRr}, t_{WRf}	ns	Figure A	—	—	20
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure A	0	—	—
	Read (RS to CS*, RD*)		ns	Figure A	10	—	—
Address hold time		t_{AH}	ns	Figure A	2	—	—
Write data setup time		t_{DSW}	ns	Figure A	20	—	—
Write data hold time		t_{H}	ns	Figure A	10	—	—
Read data delay time		t_{DDR}	ns	Figure A	—	—	150
Read data hold time		t_{DHR}	ns	Figure A	5	—	—

Table 112《[B] 16-/18-bit, High-speed write mode (HWM=1), IOVCC1=1.65V～3.10V》

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	Figure A	65	–	–
	Read	t_{CYCR}	ns	Figure A	450	–	–
Write low-level pulse width		PW_{LW}	ns	Figure A	30	–	–
Read low-level pulse width		PW_{LR}	ns	Figure A	170	–	–
Write high-level pulse width		PW_{HW}	ns	Figure A	20	–	–
Read high-level pulse width		PW_{HR}	ns	Figure A	250	–	–
Write/ Read rise/fall time		t_{WRr}, t_{WRf}	ns	Figure A	–	–	20
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure A	0	–	–
	Read (RS to CS*, RD*)		ns	Figure A	10	–	–
Address hold time		t_{AH}	ns	Figure A	2	–	–
Write data setup time		t_{DSW}	ns	Figure A	20	–	–
Write data hold time		t_H	ns	Figure A	10	–	–
Read data delay time		t_{DDR}	ns	Figure A	–	–	150
Read data hold time		t_{DHR}	ns	Figure A	5	–	–

Table 113《[C] 8-/9- bit, High-speed write mode(HWM=0/1), IOVCC1=1.65V～3.10V》

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	Figure A	60	–	–
	Read	t_{CYCR}	Ns	Figure A	450	–	–
Write low-level pulse width		PW_{LW}	ns	Figure A	30	–	–
Read low-level pulse width		PW_{LR}	ns	Figure A	170	–	–
Write high-level pulse width		PW_{HW}	ns	Figure A	20	–	–
Read high-level pulse width		PW_{HR}	ns	Figure A	250	–	–
Write/Read rise/fall time		t_{WRr}, t_{WRf}	ns	Figure A	–	–	20
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure A	0	–	–
	Read (RS to CS*, RD*)		ns	Figure A	10	–	–
Address hold time		t_{AH}	ns	Figure A	2	–	–
Write data setup time		t_{DSW}	ns	Figure A	20	–	–
Write data hold time		t_H	ns	Figure A	10	–	–
Read data delay time		t_{DDR}	ns	Figure A	–	–	150
Read data hold time		t_{DHR}	ns	Figure A	5	–	–

Clock Synchronous Serial Interface Timing Characteristics

Table 114《Normal write mode (HWM=0) / High-speed write mode (HWM=1). IOVCC1=1.65V～3.10V》

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	t_{SCYC}	ns	Figure B	100	—	20,000
	Read (transmitted)	t_{SCYC}	ns	Figure B	350	—	20,000
Serial clock high-level width	Write (received)	t_{SCH}	ns	Figure B	40	—	—
	Read (transmitted)	t_{SCH}	ns	Figure B	150	—	—
Serial clock low-level width	Write (received)	t_{SCL}	ns	Figure B	40	—	—
	Read (transmitted)	t_{SCL}	ns	Figure B	150	—	—
Serial clock rise/fall time		t_{SCr}, t_{SCf}	ns	Figure B	—	—	20
Chip select setup time		t_{CSU}	ns	Figure B	20	—	—
Chip select hold time		t_{CH}	ns	Figure B	60	—	—
Serial input data setup time		t_{SISU}	ns	Figure B	30	—	—
Serial input data hold time		t_{SIH}	ns	Figure B	30	—	—
Serial output data delay time		t_{SOD}	ns	Figure B	—	—	130
Serial output data delay time		t_{SOH}	ns	Figure B	5	—	—

RGB Interface Timing Characteristics

Table 115《18-/16- bit RGB interface (HWM=1), IOVCC1=1.65V～3.10V》

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	clock	Figure D	0	—	1
ENABLE setup time	tENS	ns	Figure D	10	—	—
ENABLE hold time	tENH	ns	Figure D	20	—	—
DOTCLK low-level pulse width	PW_{DL}	ns	Figure D	40	—	—
DOTCLK high-level pulse width	PW_{DH}	ns	Figure D	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure D	100	—	—
Data setup time	tPDS	ns	Figure D	10	—	—
Data hold time	tPDH	ns	Figure D	40	—	—
DOTCLK, VSYNC and HSYNC rise/fall time	trgbr, trgbf	ns	Figure D	—	—	25

Table 116《6-bit RGB interface (HWM=1), IOVCC1=1.65V～3.10V》

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	clock	Figure D	0	－	1
ENABLE setup time	tENS	ns	Figure D	10	－	－
ENABLE hold time	tENH	ns	Figure D	25	－	－
DOTCLK low-level pulse width	PW_{DL}	ns	Figure D	25	－	－
DOTCLK high-level pulse width	PW_{DH}	ns	Figure D	25	－	－
DOTCLK cycle time	tCYCD	ns	Figure D	60	－	－
Data setup time	tPDS	ns	Figure D	10	－	－
Data hold time	tPDH	ns	Figure D	25	－	－
DOTCLK, VSYNC and HSYNC rise/fall time	trgbr, trgbf	ns	Figure D	－	－	25

MDDI Timing Characteristics

Table 117 MDDI Receiver Timing Characteristics

《IOVCC1=1.65V～3.10V, VCC=IOVCC2=2.50V～3.10V》

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Data transfer rate	$1/t_{BIT}$	Mbps	Figure E	10	70	85
Differential transfer input skew	$\lvert\pm t_{skew\text{-}pair\text{-}I}\rvert$	ns	Figure E	－	－	0.25
Data-stb input skew	$\lvert\pm t_{diff\text{-}skew\text{-}i}\rvert$	ns	Figure E	－	－	0.3

LCD Driver Output Characteristics

Table 118

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Source driver output delay time	tdds	μs	VCC=IOVCC1=IOVCC2=3.00V, DDVDH=5.50V, VREG1OUT=5.00V, fosc=678kHz (432 line drive), Ta=25℃, REV0=0, AP=3'h3, VRH=4'h0, P0KPx=3'h0, P0KNx=3'h0, P0RNx=3'h0, P0RPx=3'h0, V0RNx=5'h0, V0RPx=5'h0, P0FPx=2'h0, P0FNx=2'h0 Same change from the same grayscale at all time-division source output pins. Time to reach the target voltage ±35mV from VCOM polarity inversion timing. R=10kohm, C=30pF	—	16	—	10
VCOM output delay time	tddv	μs	VCC=IOVCC1=IOVCC2=3.00V, DDVDH=5.50V, VREG1OUT=5.00V, fosc=678kHz (432 line drive), Ta=25℃, REV0=0, AP=3'h3, VRH=4'h0, P0KPx=3'h0, P0KNx=3'h0, P0RNx=3'h0, P0RPx=3'h0, V0RNx=5'h0, V0RPx=5'h0, P0FPx=2'h0, P0FNx=2'h0 Time to reach ±35mV when shifting between source V0⇔V31 in the worst case of scenario. R=100ohm, C=10nF	—	11	—	11

Reset Timing Characteristics

Table 119（IOVCC1=1.65V～3.10V）

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Reset "Low" level width	tRES	ms	Figure C	1	—	—
Reset rise time	trRES	μs	Figure C	—	—	10

Notes to Electrical Characteristics

Note 1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85℃.

Note 2. The following figures illustrate the configurations of input, I/O, and output pins.

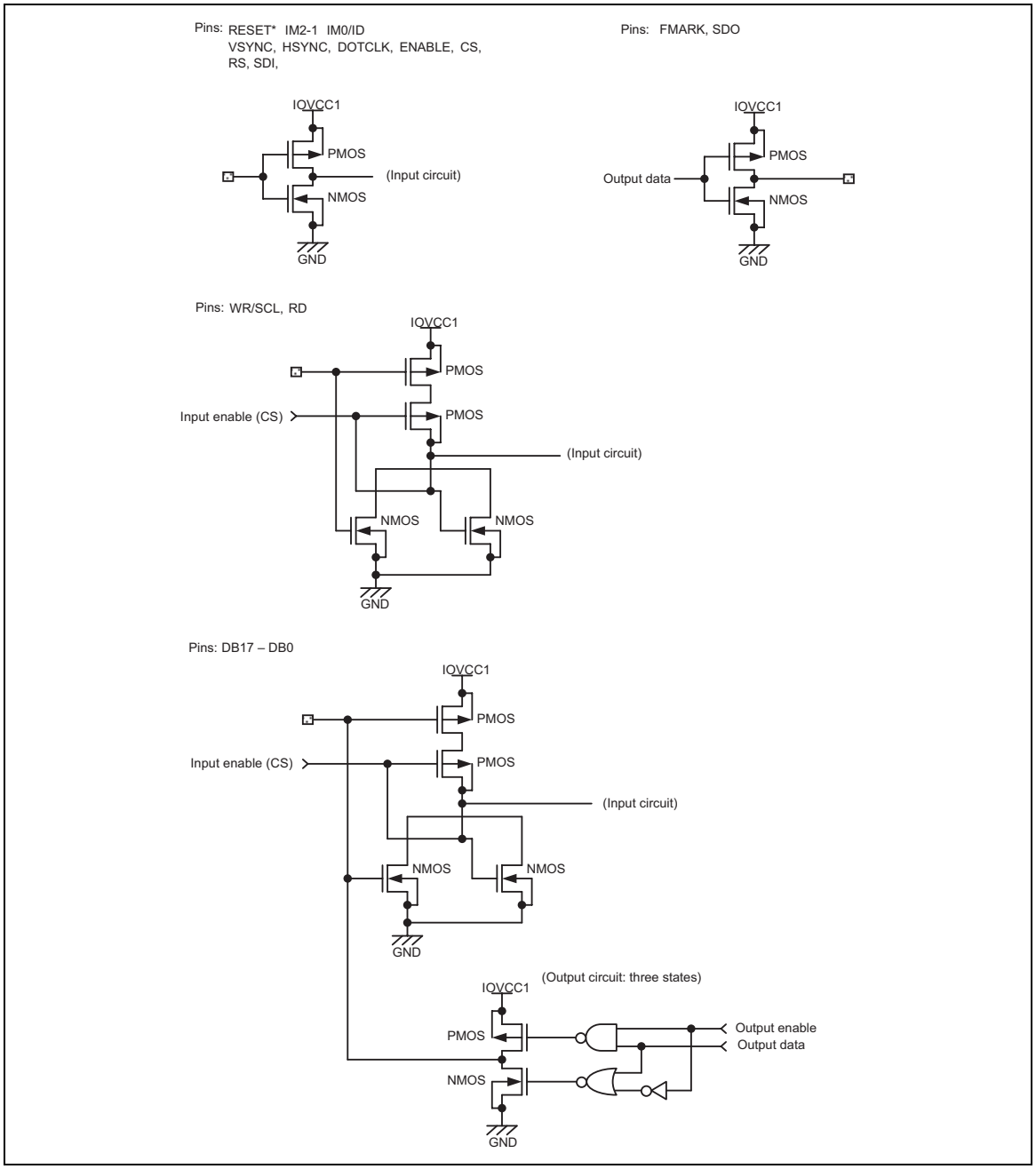


Figure 115

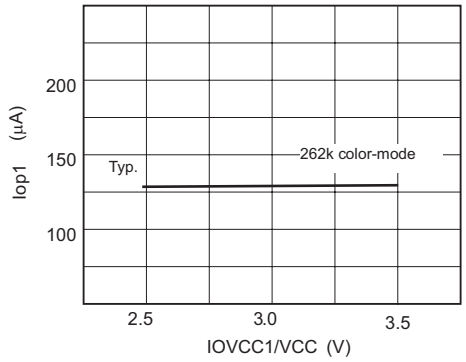
Note 3: Test 1, 2 and 3 pins must be grounded. The VDDTEST and VREFC must be fixed to AGND. The IM0/ID pin must be fixed to IOVCC1 or be grounded.

Note 4: This excludes the current in the output drive MOS.

Note 5: This excludes the current in the input/output lines. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CS* pin is high or low while not accessing via interface pins.

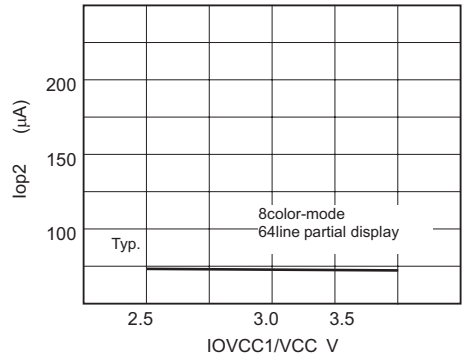
Note 6: The relationships between voltages and current consumption are as follows (reference data).

Current consumption in normal display operation (262k-color mode)



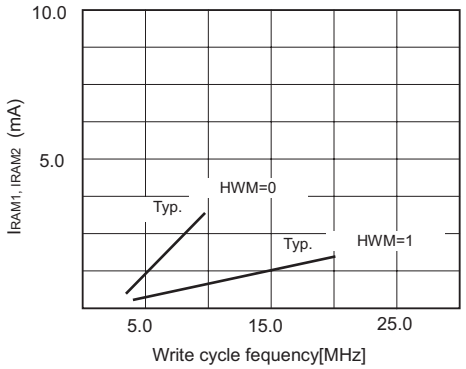
432 line
Ta=25℃, fOSC=678kHz, fFLM=60Hz,
RAM data=18'h0000
COL=0

Current consumption in normal display operation (8-color, 64 line partial display mode)



432 line
Ta=25℃, fOSC=678kHz, fFLM=40Hz,
RAM data=18'h0000
COL=1, 8-color 64 line partial display

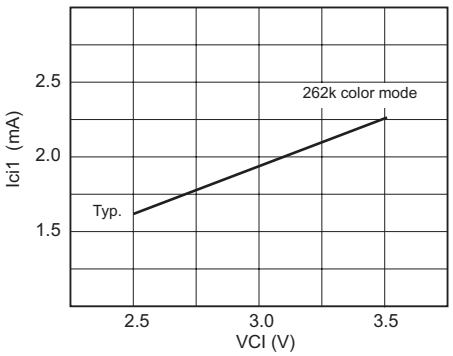
Dynamic current consumption
(RAM write during display RAM access)



IOVCC1=2.4V, VCC=3.0V
Ta=25C, fosc=678kHz

Figure 116

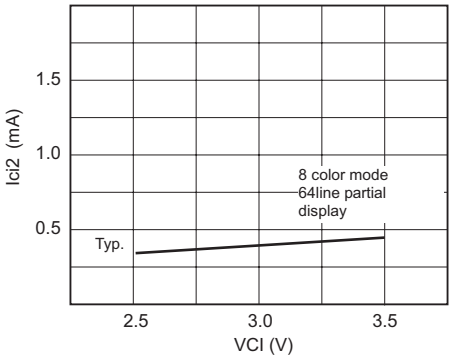
Liquid crystal power consumption in 262k-color mode (Ici1)



IOVCC1=VCC=3V, 432line,
Ta=25℃, fosc=678kHz, fFLM=60Hz,
RAM data=18'h00000,
BC0=1'h0, REV0=1'h0, COL=0,
AP=3'h3, BT=3'h5, DC0=3'h1, DC1=3'h2
VCMR=1'h1,
VC=3'h7, VRH=4'hA, VCM1=5'h1D, VDV=5'h8,
GON=1

P0KPx=3'h0, P0KNx=3'h0
P0RNx=3'h0, P0RPx=3'h0
V0RNx=3'h0, V0RPx=3'h0
P0FNx=2'h0, P0FPx=2'h0
No load on the panel

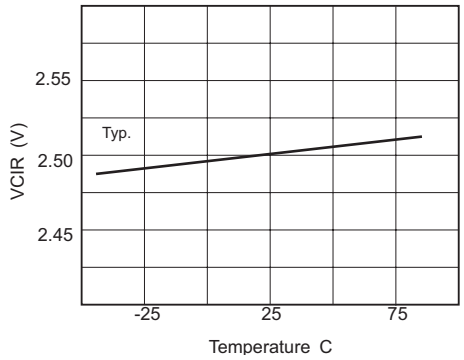
Liquid crystal consumption in 8-color, 64-line partial display (Ici2)



IOVCC1=VCC=3V, 432line,
Ta=25℃, fosc=678kHz, fFLM=40Hz,
RAM data=18'h00000,
BC0=1'h0, REV0=1'h0, COL=1,
AP=3'h3, BT=3'h5, DC0=3'h1, DC1=3'h2
VCMR=1'h1,
VC=3'h7, VRH=4'hA, VCM=5'h1D, VDV=5'h8,
GON=1,

P0KPx=3'h0, P0KNx=3'h0
P0RNx=3'h0, P0RPx=3'h0
V0RNx=3'h0, V0RPx=3'h0
P0FNx=2'h0, P0FPx=2'h0
No load on the panel

Internal Reference Voltage



VCC=IOVCC=VCI=3.00V
AP=3'h3

Figure 117

Note 7: The output voltage deviation is the difference in the voltages from adjacent source pins for the same display area. This value is shown for reference.

Note 8: The average output voltage dispersion is the variance source-output voltage of different chips of the same product. The average source output voltage is measured for each chip with same display area.

Note 9: This applies to internal oscillators when using an internal RC oscillator.

Note 10: The liquid crystal driver output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality of display on the actual panel in use.

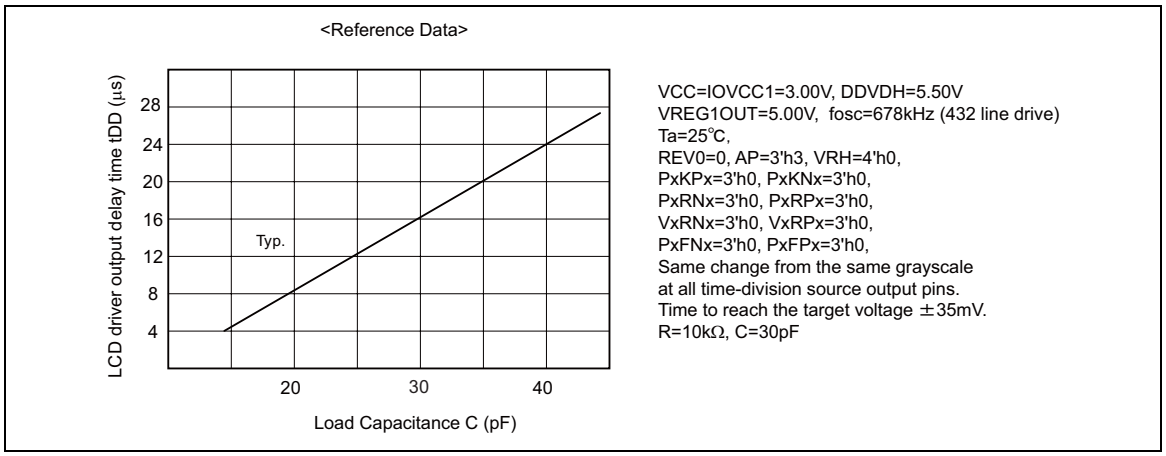


Figure 118

Note 11: The VCOM output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality of display on the actual panel in use.

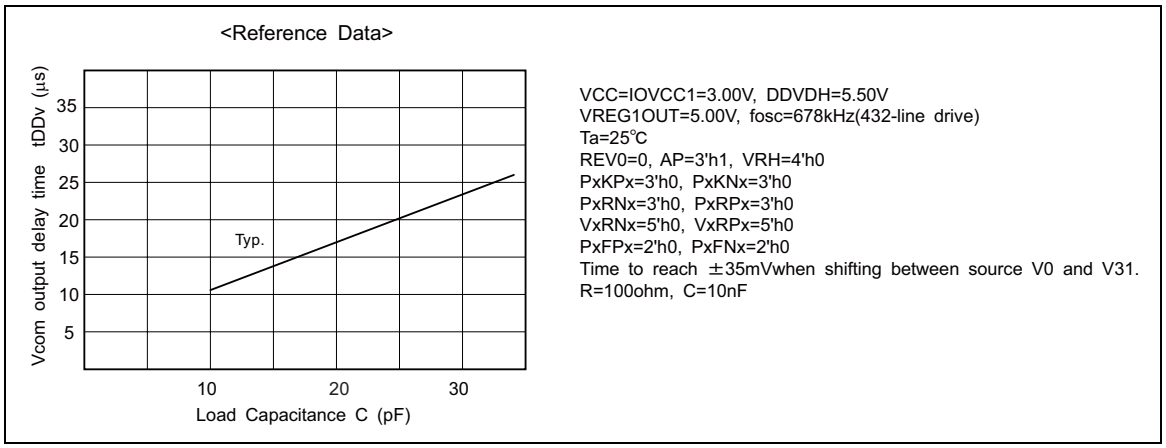


Figure 119

Note 12: Internal reference voltage VCIR depends on temperature. Following chart shows relationship between temperature and VCIR foe reference.

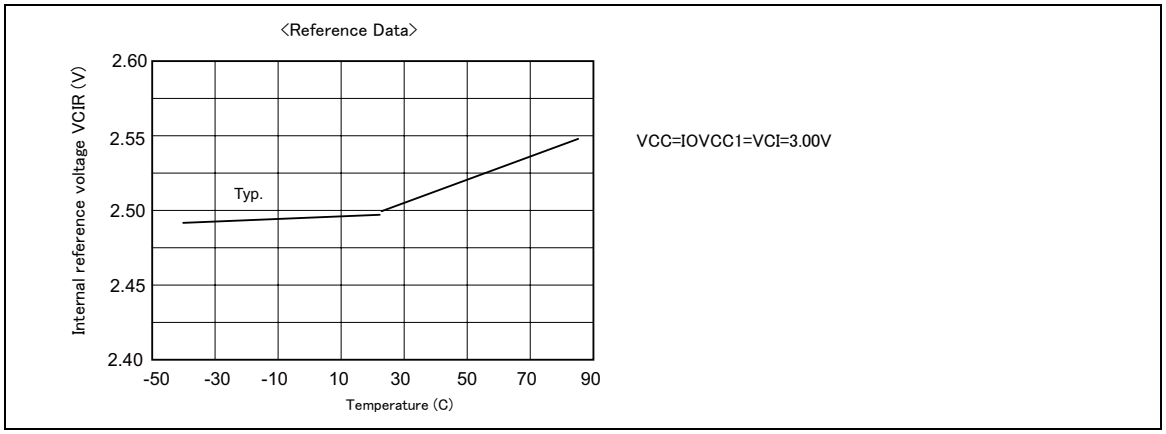


Figure 120

Test Circuits

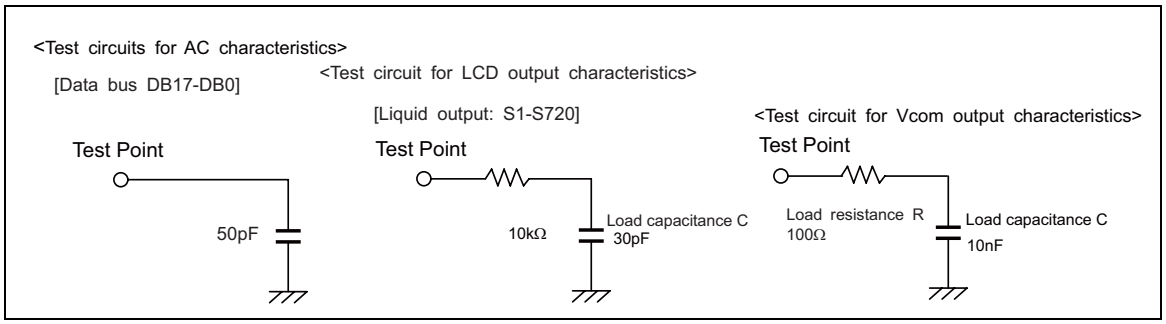
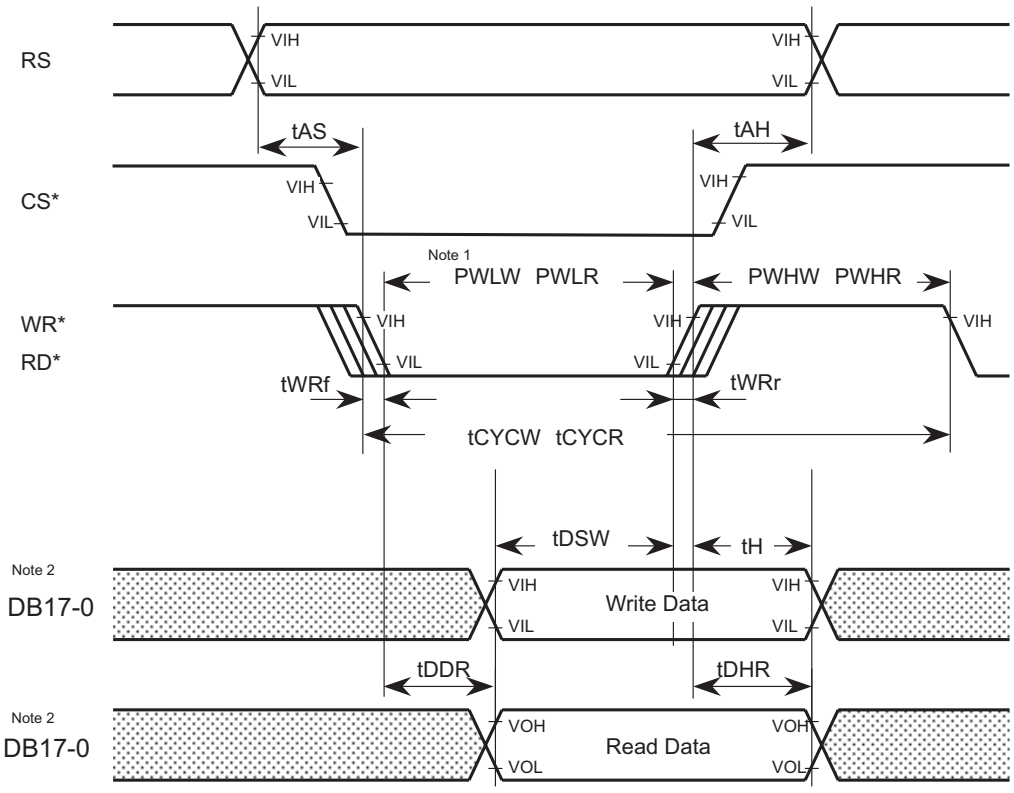


Figure 121

Timing characteristics

80-System Bus Interface



Note 1: PWLW and PWLR are defined by the overlap period when CS* is "Low" and either of WR* or RD* is "Low".
Note 2: Unused DB pins must be fixed at "IOVcc1" or "GND".

Figure A 80-System Bus Interface

Clock synchronous serial interface

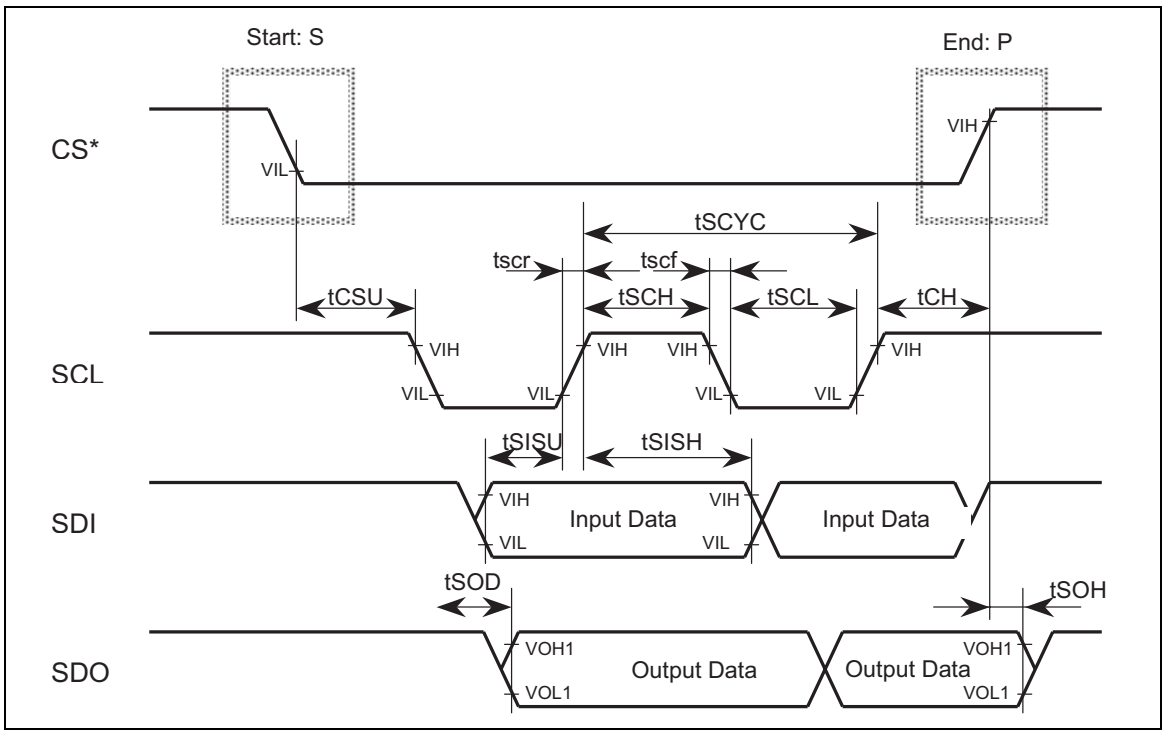


Figure B Clock synchronous serial interface timing

Reset Operation

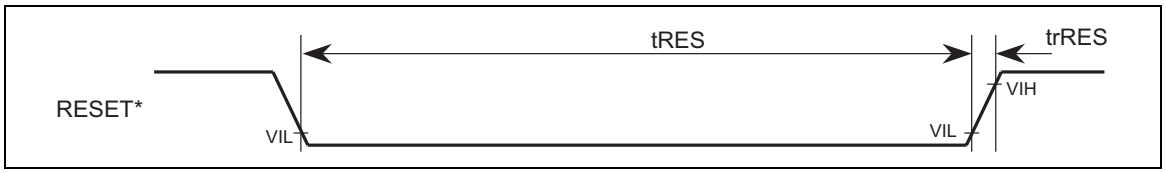


Figure C Reset Timing

RGB Interface

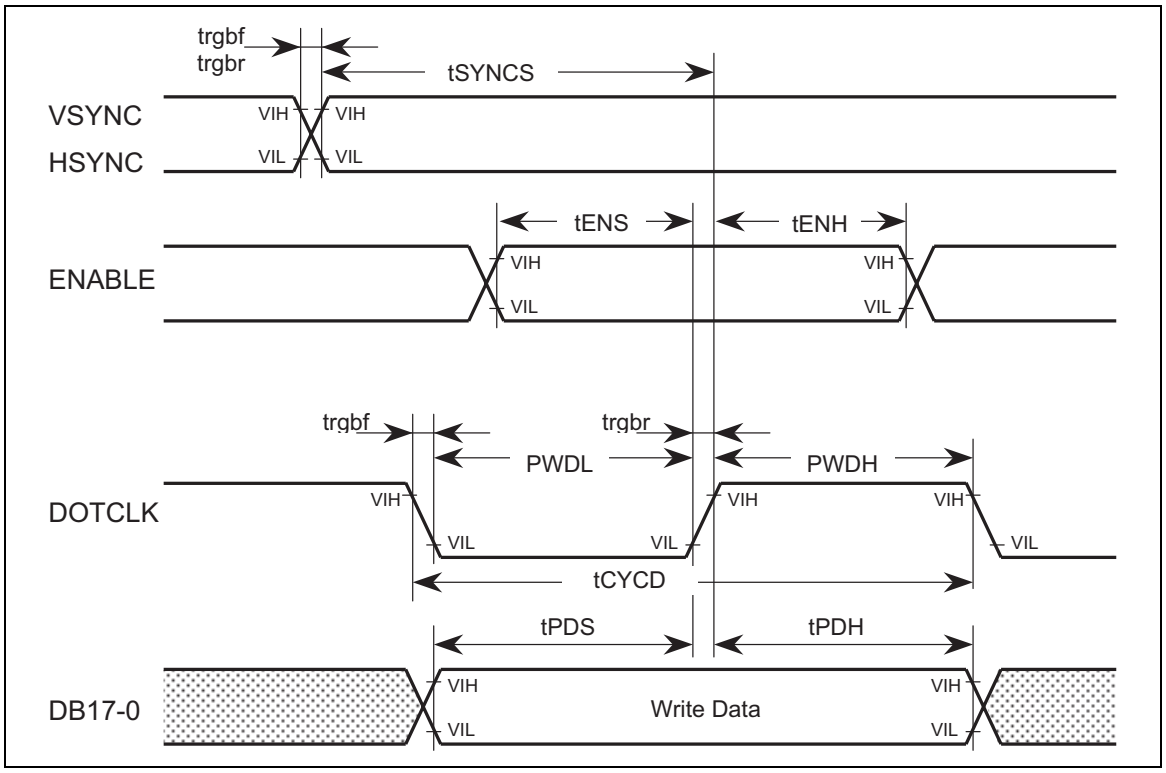


Figure D RGB Interface Timing

MDDI Input operation

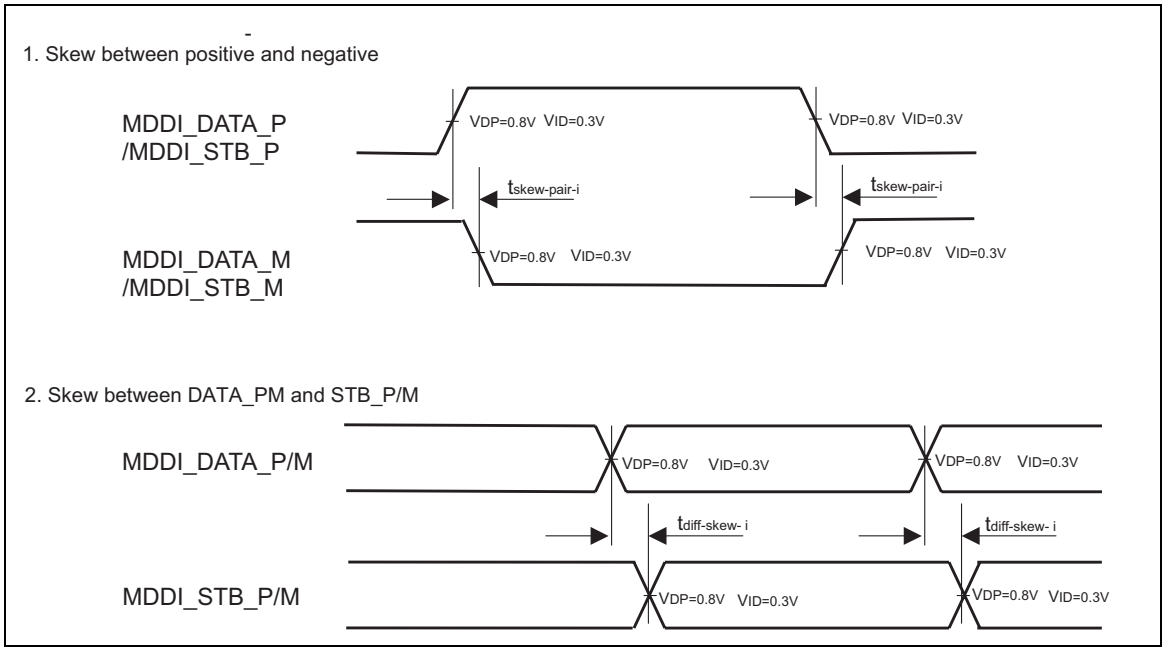


Figure E MDDI Timing

LCD Driver and VCOM outputs characteristics

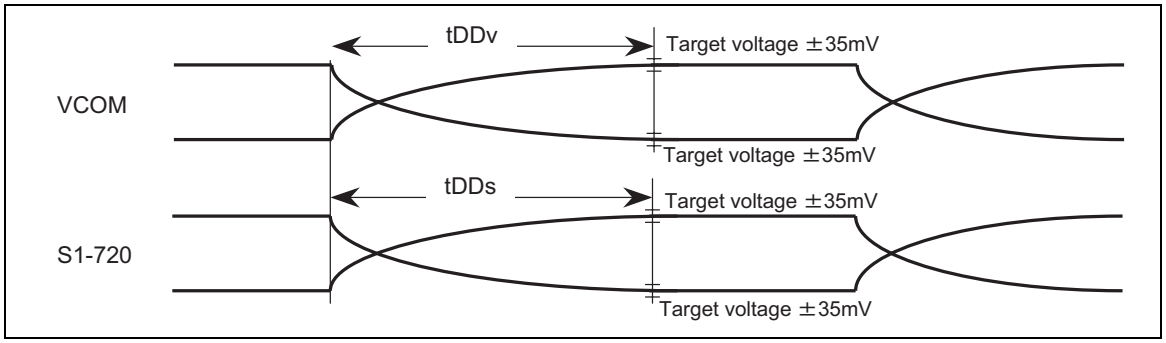


Figure F LCD Driver and VCOM Outputs Timing

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Colophon .1.0

Revision Record

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
0.11	2006.03.28		First issue		
0.12	2006.04.14	1	400 → 432		
		6	400 → 432, 216,000-byte → 232,800-byte		
		7	400-channel → 432-channel		
		8	400 output → 432 output		
			VCL → VLOUT4 (VCL)		
		9	Add VLOUT4.		
			216,800 bytes → 233,280 bytes		
		13	216,800 (240RGB x 400 (dots)) →233,280 (240RGB x 432 (dots))		
			G400 → G432		
		15	IOGND1 → GND		
			Change I/O (I/O → O) and connection (add peripheral control) of SDO.		
		16	IOVCC → IOVCC (VSYNC, HSYNC)		
			IOGND → GND		
			Add description in ENABLE and HSYNC.		
			Change I/O and connection of ENABLE and HSYNC.		
		17	IOGND → GND		
			Delete description of IOGND1.		
		19	Add description of VLOUT4, change description of VCL.		
		21	IOGND1DUM1-3 → GNDDUM1-3		
		22	IOGND → GND		
		24, 25	h18··· → h1A···		
		26	Add description of instruction data format.		
		27 ~ 71	Add description of instructions.		
		72	Add the instruction list.		
		73	Add VLOUT4, delete VCL, change IM settings		
		93, 94, 108	Change numbers to meet 432-line drive.		
		109	96’000 pixels → 103,680 pixels		
		113 ~ 118	Change numbers to meet 432-line drive.		
		120	G1-400 → G1-432		
		122	400H → 432H		
		126	IOGND1 → GND		
		132 ~ 136	Change numbers to meet 432-line drive.		
		139, 140	9’h18F → 9’h1AF, 17’h18F00 → 17’h1AF00, 17’h18FEF → 17’h1AFEF		

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
		141, 143, 145, 146	Change numbers to meet 432-line drive.		
		147 ~ 149	6'h31 → 6'h35, 400 lines → 432 lines		
		153, 154	Add VLOUT4 and "Note", change VCC- and GND-related circuit (right).		
			G1-400 → G1-432		
		156	Add "When VCOMG = 1".		
		159	Change EPROM registers.		
		161	Change EPROM Control Sequence.		
		163	IOVCC → IOVCC1, IOVCC2, 1ms → 2ms		
		166	Add the figure below the sequence.		
		167	Change COL settings (2'h1 → 1, 2'h0 → 0).		
0.1.3.1	2006.06.05	11	Description to system interface changed.		
		15	"MDDI open" added to SDO pin.		
		16	"MDDI open" added to ENABLE and HSYNC .		
		17	Table 6, pin numbers changed.		
		18	Table 8, VPP3 changed to VPP3A and VPP3B.		
		21	Table 11, pin names modified.		
		22	Pad arrangement inserted.		
		23	Inserted.		
		24-38	Pad Coordinate inserted.		
		39	Bump Arrangement inserted.		
		40	Connection Example inserted.		
		44	Device code read row of "W" deleted.		
		46	Description to EPF bits changed.		
		48-49	"Outline sharpening control" (R006h) inserted.		
		50	Note 3 to Table 15 (D[1:0]) deleted.		
		51	Description to VON changed.		
		53	Table 21, PTG[1:0] setting: "VGL fixed" changed to "Setting disabled".		
		55	VEN bit added.		
		60	Table 33 "Low power Vcom drive period" changed.		
		63	Table 38 "Source output delay period" changed.		
		65	MDDI Sub-display control (R29) inserted.		
		67	Table 44 modified.		
		68	Table 45 modified. Note 2 to Table 45 added.		
		70	Table 50 changed. Note 2 to Table 50 changed.		
		71	Description to VCOMG (R103) modified.		
		72-73	Description to DCM (R107) changed.		
		84	Description to REV (R401) modified.		
		85	Table 63 changed.		
		117	Figure 39 changed.		
		127	Figure 50 "Deep standby" changed to		

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
			"Shutdown".		
		128	Figure 51 "Deep standby" changed to "Shutdown".		
		136-137	Description and figures to "MDDI Sub-display Interface" modified.		
		151	Description to "Base image display " modified.		
		155-159	"Outline Sharpening Function" inserted.		
		166	Figure 88 Waveform modified.		
		171	Figure 91 Waveform modified.		
		172	Figure 92 Waveform modified.		
		176	Figure 96 VDDOUT added.		
		177	Figure 97 VDDOUT added.		
		178	Table 96 Pin connection to "6V" changed.		
		179	Figure 98 VCC and VLOUT4 added. LCILVL, IOVCC1 and IOVCC2's voltage changed.		
		183	Figure 101 Dummy write modified.		
		185	Figure 103 Power supply ON sequence and Power supply OFF sequence modified.		
		188	Figure 107 changed.		
		190	Target specifications and notes of Absolute Maximum Ratings added.		
		191-208	Target specifications of Electrical Characteristics, notes to Electrical Characteristics, Test Circuits and Timing Characteristics inserted.		
0.1.5	2006.06.20	All pages	EPROM→NVM		
		8	Description to NVM changed.		
		9	Table1: VPP added. Note to Table 1 deleted.		
		9, 10	Error corrected. (G1-G400 → G1-G432)		
		13	Error corrected (7 and 10).		
		16	Table 5: Function of DB0-DB17 added (MDDI).		
		18	Table 8: Note 2 to VPP3A, 3B deleted. Column of "when not in use" filled in (VPP1, VPP2, and VPP3A, 3B).		
		20	Function of VREG1OUT changed.		
		51	Table 17 changed.		
		59	Table 32 changed.		
		62	Table 37 changed.		
		67	Table 44 changed. Note 4 added.		
		69	VREG1R added. Table 50 changed.		
		83	Description to NDL0 bit changed.		
		84	Note to Table 62 changed.		
		88	Description to EAD changed. Table 66 changed. Description to EOP changed.		
		89	Instruction list changed.		
		90	Error corrected (VLOUT2, output pin initial state).		
		111	Error corrected. (Figure 32: 400 lines→432 lines. Figure 33: 432 lines → 392 lines.)		

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
		117	Sub-Display Interface RAM Write Sequence: “18-/16-bit” added.		
		119	Table 79, Single Access: Description changed.		
		120	Figure 42: Bit changed.		
		121	Figure 43: Bit changed.		
		123	Table 81: Bit changed.		
		124	Table 82: Bit changed.		
		128	Figure 51: Error corrected.		
		129	Figure 52: Error corrected.		
		140	Figure 62: Error corrected.		
		175	Figure 94: Error corrected. (γ curve, negative polarity. P0RP1→P0RN1, P0KP3→P0KN3)		
		176	Figure 96: Error on VCILVL corrected.		
		177	Figure 97: Error on VCILVL corrected.		
		185	Figure 103 (Power supply ON/OFF sequence): modified.		
		190	Table 101: Maximum value of VGH-VGL (power supply voltage 8) added.		
		191	Table 102 :VCC range : VCC=2.50V~3.30V → VCC=2.50V~3.10V Current consumption for shutdown mode: IOVCC=1=2.40V, VCC=3.00V → IOVCC1=IOVCC2=3.00V		
		192	VCI=3.00V → VCI=2.50V, VDV=5’h8 → VDV=5’h1A		
		193	VCC=2.50V~3.30V → VCC=2.50V~3.10V		
0.1.6	2006/09/06	9	Table 1: NVM_FUSE → NVM, Error correction (VLOUT1 VCI x2, x3 → VCI x2)		
		10	Figure 1 (VREG1OUT ←→) → (VREG1OUT←). Error correction (VPP1-3 → VPP1-2, VPP3A, 3B)		
		12	Table 4 80-system 8-bit interface: 3-transfer added (1st: 2 bits, 2nd: 8 bits, 3rd: 8 bits).		
		19	Error correction (VCI: VLOUT4 added)		
		45	R002 Instruction list: Error correction.		
		51	Table 17 VCOML → GND		
		66	R100 Instruction list: Error correction (STB deleted).		
		71	Table 52 VCOML → GND		
		73	Table 54 changed. “When DCM[1]=1, step-up reference clock that generates every 1H period is set at 16 clocks” added.		
		86	Table 64: Note added.		
		88	“Software Reset (R600h)” added.		
		100	Figure 16: EPE=2’h0 added (RAM data write).		
		105	Figure 25: EPE=2’h0 added (RAM data write).		
		143	Figure 64: Error correction.		

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
		144	Figure 65: Error correction.		
		184	Figure 101: VPP1=9.0±0.3V (TBD) → VPP1=9.0 ±0.1V (TBD), VPP2=7.0V±0.3V(TBD) → VPP2=7.5V±0.1V(TBD)		
		186	Figure 103: SAP → SAP=1, VCM → VCOMG=1 (Power supply ON sequence)		
		189	Figure 106 revised.		
		190	Figure 107 inserted.		
		191	Figure 108 inserted.		
		197	Table 107 [A] 1-/ 2-/ 3- transfer mode → [A] 3-transfer mode		
		202	Figure 111 revised.		
		208	Figure 117 Note 1 → Note 2, Note 2 → Note 1, VIH → VOH, VIL → VOL.		
		209	Figure 118 Error correction (headline)		
		211	Figure 122 Error correction (S1-240 → S1-720)		
0.1.7	2006/11/15	14	Set the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module. → Set the optimal gate driver scanning mode for the module in combination with the GS bit.		
		18	Error correction. (GND: Internal logic GND → GND for internal logic and interface pins (RESET, CS, WR, RD, RS, DB15-0, VSYNC, HSYNC, DOTCLK and ENABLE).)		
			Revise description. (IOVCC1, IOVCC2: if VCC, IOVCC1 =IOVCC2 → when VCC = IOVCC1 = IOVCC2).		
		21	Error correction. (TEST1-3: Connect to IOGND → Connect to GND).		
		45	Error correction. (B/C bit: Delete “when EOR=1”, “In either liquid crystal drive method, the polarity inversion is halted in blank period (back and front porch periods)”).		
			Error correction (NW bit: Sets “n” for the number of lines from 1 to 64 → Sets “n” for the number of lines from 1 to 4)		
		47	Table 14 Error correction.		
		50	Error correction. (Note 2 to Table 15, PTS[2:0] → NDL0.		
		55	COL description: Error correction. (VREG1OUT/GND → V0/V31)		
			Revise VEM description.		
		62	Error correction. (Note 3 to Table 37: The reference point is where SFTCLK rises when the rising position is set to 0 clock. → The reference point is falling edge of gate control signals.)		
		63	Error correction (FMP bit, amplitude: IOVCC1-IOGND → IOVCC1-GND, Setting range: 9’h000 ≤		

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			FMP ≤ BP + NL + FP → 9'h000 ≤ FMP ≤ BP + NL + FP – 1)		
		65	Error correction (MDDI Sub-display Control (R029h) → (R092h)		
		66	DSTB description: Add "GND level is outputted to the panel in the shut down mode."		
		78	Figure 7 Error correction. (Delete HAD and VAD).		
		79	UID description: Revised.		
		81	Figure 8, Note 3: Delete HAD, VAD.		
		85	Error correction. (VL0 description: NL0[5:0] → VL0. Delete "Make sure NL0[5:0] ≤ 432.")		
		97	Add "262,144 colors is 8-bit 3-transfer mode" (Note 2 to Table 69).		
		104	Error correction. (The unused DB pins must be fixed at either IOVCC or IOGND level → The unused DB pins must be fixed at either IOVCC1 or GND level).		
		111	Error correction. (Internal clock frequency (fosc) and RAMWriteSpeed equation: 16 (clocks) → 23 (clocks)). Delete "external resistors and" from Note 2 to internal clock frequency example.		
		135	Error correction (Internal clock frequency equation: 16 (clocks) → 23 (clocks))		
		139	Error correction. (Figure 61: Bus width 9 → 3)		
		150	Error correction. (Figure 70: Set index register to R22h → R202h)		
		162	Table 94: Delete line of "Write mask function".		
		169	Error correction: Number of clocks per line: RTN bit → Number of clocks per line: RTNI bit		
		179	Error correction (Table 97: (13) VLOUT3 → (14) VLOUT3)		
		180	Error correction (Figure 98, When VREG1R=1 → VREG1R=0). Error correction (Note 1, VGH-VGL ≤ 25V → VGH-VGL ≤ 28V).		
		182	Error correction. (2nd paragraph)		
		194	Table 102 Current consumption RAM access mode 1, tCYCW=150ns → 110ns, delete VCM1=5'h1D, AP=2'h3. Current consumption RAM access mode 2, tCYCW=75ns → 80ns, delete VCM1=5'h1D, AP=2'h3.		
		195	Table 102 Ici1: VC=3'h7 → 3'h1, Ici2: VC=3'h7 → 3'h1.		
		197	Table 107 tCYCW (min.) 150 → 110, PWLW		

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			(min.) 55 → 30. PWHW 70 → 30, tDSW 25 → 20.		
		198	Table 108 PWLW (min.) 35 → 30, PWHW 35 → 20, tDSW 25 → 20.		
			Table 109 tCYCW (min.) 55 → 60, PWLW (min.) 35 → 30, PWHW 18 → 20, tDSW 25 → 20.		
		199	Delete Table 110 ([D] Write mode except [A], [B] and [C]).		
		201	Table 114 tddv: Time to reach ±35mV when shifting between source V0⇔V31. → Time to reach ±35mV when shifting between source V0 ⇔V31 in the worst case of scenario.		
		203	Error correction. (Add Note 6)		
		204	Figure 112 Error correction (Dynamic current consumption graph: Add IOVCC=2.4V, VCC=3.0V, Ta=25C, fosc=678kHz).		
0.18	2007/02/06	13	Oscillator: TBD kHz → 678kHz		
		18	IOVCC2: Add “Connect to power supply when MDDI is not used.”		
			IOGND2: Error correction. ((IOVCC2=0V → IOGND2 =0V). Add “Connect to GND when MDDI is not used”.		
		41-42	GRAM address map, Table 12, 13: Error correction.		
		60	Error correction. VEQWI IB10-9 → IB9-8		
		61	Change Table 34.		
		67	DSTB bit description revised.		
		74	DCM bit description: Error correction. RTNE ≤ 6’h1F → 7’h1F, RTNE ≥ 6’h20 → 7’h20, RTNE ≥ 6’h20 → 7’h20.		
		80	Instruction table: Error correction. (R290h → R281h)		
		112	Delete “T.B.D” (Internal clock frequency)		
		131	Figure 52: Delete “T.B.D” (1ms or more).		
		133	MDDIdataTransferSpeed(min.) < MDDIdataTransferSpeed ≤ T.B.D → 85Mbps		
		134	Delete “T.B.D”		
		136	MDDIdataTransferSpeed(min.) < MDDIdataTransferSpeed ≤ T.B.D→ 85Mbps		
		168	Description revised. Note added.		
		169	Error correction (Note deleted).		
		170	fosc: 678 kHz (T.B. D) → fosc: 678 kHz (delete T. B. D.)		
		176	Table 96: Error correction. (P0FP1/P0FN2, P0FP3 / P0FN0)		
		183	Description revised. (2nd paragraph)		
		185	Figrue 101: Delete “T. B. D”.		
		187	Figure 103 Delete “T.B.D”.		

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		188	Figure 104: Error correction. (Display OFF sequence → Display ON sequence, LCD power supply ON sequence → LCD power supply OFF sequence)		
		194	Note 4 added.		
		195-202	Electrical characteristics: overall revision.		
		196	Differential input “High” level voltage → Differential input “High” threshold voltage (VIT+), Differential input “Low” level voltage → Differential input “Low” threshold voltage (VIT-), Differential input “High” level voltage → Differential input “High” threshold voltage (VIT+off), Differential input “Low” level voltage → Differential input “Low” threshold voltage (VIT-off)		
		198	Table 106 (clock characteristics): Error correction. Delete “Internal RC oscillator, Ta=25℃”.		
		205	Figure 112: TBD → Revised.		
		206	Figure 113: TBD → Revised.		
		208	Figure 114, 115: TBD → Revised.		
1.00	2007/04/20	6	Description: Also, the R61509 incorporates step-up circuit and voltage follower circuit to generate TFT liquid crystal panel drive voltages. → The power supply circuit incorporates step-up circuit and voltage follower circuit to generate TFT liquid crystal panel drive voltages.		
		9	Table 1: VPP3: GND → VPP3A/VPP3B: GND		
		12	The R61509 allows switching interface by instruction according to the display, i.e. still and/or moving picture(s). The R61509 writes all display data via RGB interface to the internal GRAM in order to transfer data only when updating the data and thereby reduce the data transfer and power consumption for moving picture display. → The R61509 allows switching interface by instruction according to the display, i.e. still and/or moving picture(s) in order to transfer data only when the data is updated and thereby reduce the data transfer and power consumption for moving picture display.		
		18	Table 120 Power Supply Pins: VPP3A, 3B, when not used GND/Open → GND.		
			Note 1 deleted.		
		43	Instruction: “The R61509 starts internal processing after storing control information of *externally* sent data (18, 16, 9, 8, 1 bit(s)) in the instruction register (IR) and the data register (DR).” → “The R61509 starts internal processing after storing control information (18, 16, 9, 8, 1 bit(s)), *sent from the microcomputer*, in the instruction register (IR) and the data register (DR).”		
			“When accessing the R61509’s internal RAM,		

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			data is processed in units of 18 bits" deleted.		
		45	R002h NW[1:0]: Sets "n" for the number of lines from 1 to 4 to set the interval of inverting the polarity of C-pattern waveform when B/C = "1". → Sets "n" for the number of lines from 1 to 4 to set the interval of inverting the polarity of *line inversion drive* (C-pattern waveform) when B/C0 = 1		
		47	Figure 4: Error correction. (17'h13FEF → 17'h1AFEF)		
		48	Figure 5: Error correction. (17'h13FEF → 17'h1AFEF)		
		51	Table 17 (VON bit): AP[1:0]→AP[2:0]		
		56	DM[1:0] Delete "Selects the interface for the display operation."		
		58	R010h RTNI: Note to Table 29 added.		
		62	R020h DIVE Table 35 8-bit x 3 transfers RGB Interface → 6-bit x3 transfers RGB Interface		
		67	R100h: AP[1:0]→[2:0]. Description to AP bit: "In no-display period, set AP1-0 = 2'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption." → "In no-display period, set AP[2:0]=3'h0 to reduce power consumption. Set AP[2:0]=3'h7 and SAP[1:0]=2'h3 when VP is not 3'h7." Table 42 changed. Notes to Table 42 added.		
		68	R100h: SAP[1:0] bit added.		
		69	Note to Table 46 deleted.		
			Note 3, 4 to Table 47 are added.		
		70	R102h VRH: Note 2 to Table 50 added.		
		72	R103h: Table 52 AP[1:0] → AP[2:0]		
		75	R112h Power Control 7 (TBT bit) added.		
		77	Table 56 Note: (Vn+Vn+1)/2, (Vn+2Vn+1)/3 → (Vn+Vn+1)/2 ,(V1+2V0)/3, (Vn+2Vn+1)/3		
		78	Table 57 Note: (Vn+Vn+1)/2, (Vn+2Vn+1)/3 → (Vn+Vn+1)/2, (V1+2V0)/3, (Vn+2Vn+1)/3		
		79	RD[17:0] "the first word read immediately after RAM address set is executed is taken in the internal read-data latch and invalid data is sent to the data bus" → "the first word read immediately after RAM address set is not outputted, so that it is invalid"		
		82	VSA, VEA: "See GRAM Address Map." added.		
		91	Instruction List Rev 0.0.5.2 →0.0.5.4		
		92	I.2 instruction from the MPU→ instruction from the microcomputer		
		97	FMARK interface operation added.		
		115-118	FMARK Interface inserted.		
		156	"For this reason, there is no need to take the mounting position of the panel into consideration when designing a display on the panel." deleted.		

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		182	Figure 100 (13) diode: VCI-VGH → DDVDH-VGH		
		183	Figure 101 (13) diode: VCI-VGH → DDVDH-VGH. Note 2 added in the Figure.		
		190	Figure 107: RTNI, DIVI added to Instruction initial setting (User setting 2). R112h TBT[1:0]=2'h0 added to LCD Power supply ON sequence. BT=3'h7 and VC=3'h4 or 6 added to Power supply user setting. Note 1 and 2 added.		
		191	Figure 108 Display ON/OFF Sequences: "Power supply user setting R100h: BT / R101h: VC added."		
		193	Figure 110 Shutdown Mode IN/EXIT Sequences: "User setting NL, BP, FP, Gamma, RTNI, DIV, others" added next to Initial instruction setting.		
		194	Figure 111 "User setting NL, BP, FP, Gamma, RTNI, DIV, others" added next to Initial instruction setting.		
		195	Figure 112 "User setting NL, BP, FP, Gamma, RTNI, DIV, others" added next to Initial instruction setting.		
		198-211	Electrical Characteristics, Notes to Electrical Characteristics: Gamma adjustment register names VxRPx → V0RPx, et al.		
		198-120	Table 104 DC Characteristics: AP=2'h3→3'h3.		
		200	Table 106 Step-up Circuit Characteristics: AP=2'h3→3'h3.		
		205	Table 116 LCD Driver Output Characteristics: AP=2'h3→3'h3.		
1.01	2007/04/23	18	Table 121 Power Supply Pins: VPP3A, 3B Note 1 deleted.		
		40	Connection Example Rev 1.0.2→ 1.0.3 (diode: VCI-VGH → DDVDH- VGH)		
		89	R600h SRST: "When software reset is executed, instruction registers other than SRST, UID[3:0], VCM1[4:0], VCM2[4:0] and VCMSEL are initialized." added.		
		94	Figure 9 Basic Mode Operation of the R61509: Software reset added.		
		98	"See also i80-i/F Endian Control (R606h) for the order of receiving data when data is transferred in multiple times" added.		
		137	internal oscillation frequency for writing QVGA→ WQVGA		
		145	(Title) External Display Interface → RGB Interface		
		154	Notes to External Display Interface Operation → Notes to RGB Interface Operation.		
			Table 91 Functions Not Available in External Display Interface operation → Functions Not Available in RGB Interface operation		
		196	Figure 113 Error correction: R007h → R00Bh		

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			Figure 114 Error correction: R007h → R00Bh		
		209	Figure 117 AP=2'h3 → 3'h3		
1.02	2007/08/09	8	VGH-GND = 10.0V ~ 15.0 V → 10.0V ~ 15.5 V		
		10	Table 1:VGH=10.0V ~ 15.0 V → 10.0V ~ 15.5V.		
		19	Table 8 VPP3A/VPP3B NVM Read: GND / Open → GND		
		20	VLOUT2 = max 15.0V → max. 15.5V		
		41	Connection Example Rev 1.0.3 (2007. 04. 18) → Rev 1.0.4 (2007.06.29)		
		47	R003h Entry Mode: DFM description added.		
		61	R012h Panel Interface Control 3: SEQWI bit added.		
		65	R022h Panel Interface Control 6: SEQWE bit added.		
		69	R100 Power Control 1, AP bit: Error correction (VP → VC)		
		70	Table 46, Note 3: VGH = max 15.0V → max 15.5V. VCL = max-3.0V added.		
		114	Calculation example: Internal clock frequency (fosc) [Hz] = 678kHz x 1.1/1.0=746kHz → 678kHz x 1.07/1.0=726kHz.		
			Note 1: ±10% → ±7%		
			Minimum speed for RAM writing [Hz] > 240 x 432 / {((14 + 432 – 2) lines x 23 clocks) x 1 / 746 kHz} = 7.6MHz → > 240 x 432 / {((14 + 432 – 2) lines x 23 clocks) x 1 / 726 kHz} = 7.4MHz		
		115	Figure 32: RC oscillation ±10% → ±7%, RAM write 7.0MHz→ 7.4MHz		
			Figure 33: RC oscillation ±10% → ±7%, RAM write 7.1MHz→ 7.4MHz		
		118	Calculation example: Internal clock frequency (fosc) [Hz] = 678kHz x 1.1/1.0=746kHz → 678kHz x 1.07/1.0=726kHz.		
			Minimum speed for RAM writing [Hz] > 240 x 432 / {((14 + 432 – 2) lines x 23 clocks) x 1 / 746 kHz} = 7.6MHz → > 240 x 432 / {((14 + 432 – 2) lines x 23 clocks) x 1 / 726 kHz} = 7.4MHz.		
		119	Figure 37: RC oscillation ±10% → ±7%, RAM write 7.6MHz→ 7.4MHz		
		140	Internal oscillation frequency: Internal clock frequency (fosc) [Hz] = 678kHz x 1.1/1.0 = 746kHz → 678kHz x 1.07/1.0 = 726kHz.		
			Note 1: ±10% → ±7%		
			MDDIdataTransferSpeed (min.) = 1,872,464 (bits) / (14+432+3+14+432-14-2) x 23 (clocks) x 1 / 746 (kHz) –1 (ms) = 72 (Mbps) → = 1,872,464 (bits) / (14+432+3+14+432-14-2) x 23 (clocks) x 1 / 726 (kHz) –1 (ms) = 70 (Mbps)		
		143	Internal oscillation frequency: Internal clock frequency (fosc) [Hz] = 678kHz x 1.1/1.0 =		

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			746kHz → 678kHz x 1.07/1.0 = 726kHz.		
			Note 1: ±10% → ±7%		
			MDDIdataTransferSpeed (min.) = 1,872,464 (bits) / {1/60 + (14 + 432-2) x 23 (clocks) x 1 / 746 (kHz) – 1 (ms)} = 64 (Mbps) → = 1,872,464 (bits) / {1/60 + (14 + 432-2) x 23 (clocks) x 1 / 726 (kHz) – 1 (ms)} = 63 (Mbps)		
		156	Table 93: Error correction. (External Display Interface → RGB Interface)		
		184	Figure 100: Diode symbol revised.		
		185	Figure 101: Diode symbol revised.		
		186	Table 102: (13)VCI-VGH → DDVDH-VGH		
		187	Figure 102 (Voltage Setting Pattern Diagram): voltage values deleted.		
		192	Power Supply Instruction Setting: Description added.		
		193	"Notes to Power Supply ON Sequence" inserted.		
		200	Table 105 Absolute Maximum Ratings: Power Supply 9~11, NVM write temperature added.		
		203	Table 109 (Internal reference voltage): Note 12 added.		
		204	Table 110 (Clock characteristics): Min. 611 → 631, Max. 745 → 725		
		213	Figure 118: Error correction. (AP=2'h3→ 3'h3)		
			Figure 119: Error correction. (AP=2'h1→ 3'h1)		
		214	Note 12 added.		
		215	Figure A 80-System Bus Interface: Error correction. (tWRr→ tWRf)		
1.03	November 26, 2007	8	VGH-GND = 10.0V ~ 15.5 V → 10.0V ~ 17.5V		
		10	Table 1 VGH 10.0V ~ 15.5 V → 10.0V ~ 17.5V		
		20	Table 9 VLOUT2 = max 15.5V → max 17.5V		
		70	Note 3 VGH = max. 15.5V → max 17.5V		
		185	Added "Make sure that VCI≤ 3.0V."		
		186	Recommended diode: HSC226 → HS*226		
		204	Table 111 tWRr, WRf Max 10→20		
		205	Table 112, 113 tWRr, WRf Max 10→20		